

MIDAS, PROTOTYPE MULTIVARIATE INTERACTIVE DIGITAL ANALYSIS SYSTEM — PHASE I

Volume III: Wiring Diagrams

by

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16. Abstract <p>The MIDAS System is a third-generation, fast, multispectral recognition system able to keep pace with the large quantity and high rates of data acquisition from present and projected sensors. MIDAS, for example, can process a complete ERTS frame in forty seconds and provide a color map of sixteen constituent categories in a few minutes. A principal objective of the MIDAS Program is to provide a system well interfaced with the human operator and thus to obtain large overall reductions in turnaround time and significant gains in throughput. This goal is elaborated in this report as an objective of the Phase II program.</p> <p>This report describes the hardware and software generated in Phase I of the overall program. The system contains a mini-computer to control the various high-speed processing elements in the data path and a classifier which implements an all-digital prototype multivariate-Gaussian maximum likelihood decision algorithm operating at 2×10^5 pixels/sec. Sufficient hardware has been developed to perform signature extraction from computer-compatible tapes, compute classifier coefficients, control the classifier operation, and diagnose operation.</p> <p>Volume I describes the MIDAS System in detail; Volume II contains the diagnostic programs used to test MIDAS' operation; Volume III displays the MIDAS construction and wiring diagrams.</p>					
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PREFACE

A comprehensive multispectral program devoted to the advancement of state-of-the-art techniques for remote sensing of the environment has been a continuing program at the Environmental Research Institute of Michigan (ERIM), formerly the Willow Run Laboratories of The University of Michigan. The basic objective of this multidisciplinary program is to develop remote sensing as a practical tool to provide the user with processed information quickly and economically.

The importance of providing timely information obtained by remote sensing to such people as the farmer, the city planner, the conservationist, and others concerned with problems such as crop yield and disease, urban land studies and development, water pollution, and forest management must be carefully considered in the overall program. The scope of our program includes: (1) extending the understanding of basic processes; (2) discovering new applications; (3) developing advanced remote-sensing systems; (4) improving fast automatic data processing systems to extract information in a useful form; and also (5) assisting in data collection, processing, analysis and ground truth verification. The MIDAS program applies directly to No. (4) with its improved data processing capability.

This document is the final report for Phase I of the MIDAS program under NASA Contract NAS1-11979 and covers the period from October 1972 through February 1974. The contract effort was monitored by Mr. William Howle of NASA-Langley. The overall program is guided by Mr. R. R. Legault, Vice President of ERIM, and Director of the Infrared and Optics Division. Work on this contract was directed by J. D. Erickson, Head of the Multispectral Analysis Section, and by F. J. Kriegler, Principal Investigator. The ERIM number for this report is 195800-25-F.

ERIM personnel who contributed to this project and who co-authored this report are Dempster Christenson, Michael Gordon, Roland Kistler, Seymour Lampert, Robert Marshall, and Rowland McLaughlin. In addition to providing the text, their individual contributions were as follows: Dempster Christenson and Michael Gordon provided system programming and diagnostic software; Roland Kistler and Seymour Lampert provided the detailed design and performed system checkout; Robert Marshall aided in overall system configuration; Rowland McLaughlin organized this report. The authors wish to acknowledge the direction provided by Mr. R. R. Legault and Dr. J. D. Erickson. Outstanding contributions were made by the following persons: John Baumler, Clyde Connell, William Juodawlkis, Robert Pierson, Cary Wilson, and Nancy Wilson for their efforts in system construction.

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MIDAS, PROTOTYPE MULTIVARIATE INTERACTIVE DIGITAL ANALYSIS
SYSTEM—PHASE I

Volume III: Wiring Diagrams

1

INTRODUCTION

This volume contains block diagrams and schematics detailing the construction of the MIDAS Classifier. Their organization forms a tree structure in which the more general block diagrams reference the more detailed block diagrams which lead to the schematics. This provides a self-explanatory set of diagrams enabling the reader to acquaint himself with system design and circuitry to any desired level of detail.

2

GENERAL SYSTEM CONFIGURATION

The Phase-I MIDAS System is most easily visualized if organized into subsystems as shown in the block diagram of Fig. 1. The system is under complete control of the Digital Equipment Corporation (DEC) PDP-11/45 computer system. All control inputs by an operator are made by way of the computer keyboard. All commands are translated by computer software into code words and sent out over interface devices to set up the hardware registers in the special-purpose processor. These codes are decoded in three of the blocks shown in Fig. 1. These three places are: (1) in the control section, (2) in the clock section, and (3) in the Diagnostic/Output section. These codes will be described in detail in subsequent sections.

The MIDAS System is housed in one 6-foot rack. The physical location of the major components is shown in Fig. 2. Each of the 4 quadratic pipes is housing in a wire-wrap card file containing 13 wire-wrap circuit boards. The quadratic calculation is accomplished by a set of 12 boards in each bay while the other board in each bay is different as shown in Fig. 2.

High-speed mass data is transferred to and from the computer by means of (1) the A/D-D/A (hybrid) section, (2) the clock section, and (3) Diagnostic/Output section. High-speed multichannel data is transferred through the hybrid section and the quadratic computation pipes. The figure numbers shown in each of the blocks of Fig. 3 refer to more detailed figures describing that block.

The control bay and the hybrid bay have room for 22 circuit boards. There are 20 boards in the control bay numbered C-1 through C-20. There are 19 boards in the hybrid file numbered H-1 through H-19.

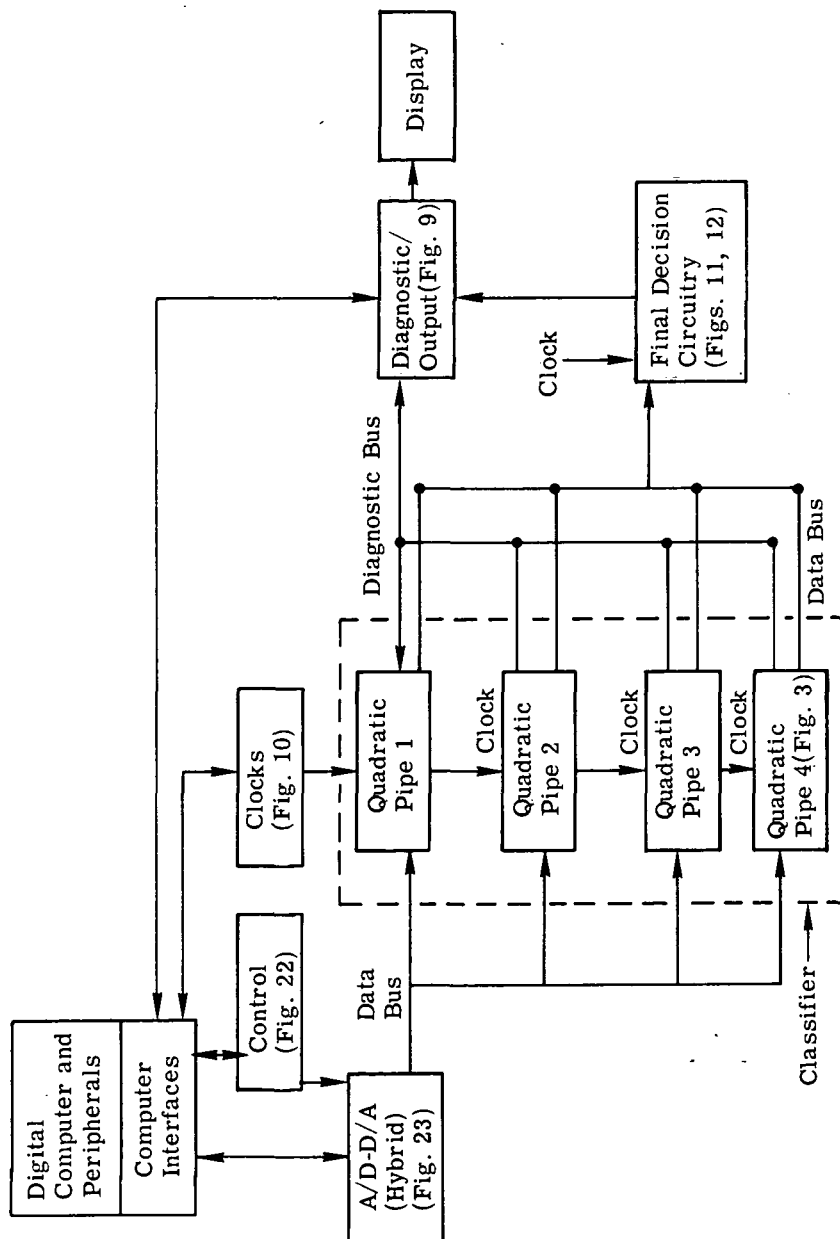


FIGURE 1. BLOCK DIAGRAM OF THE MIDAS SYSTEM

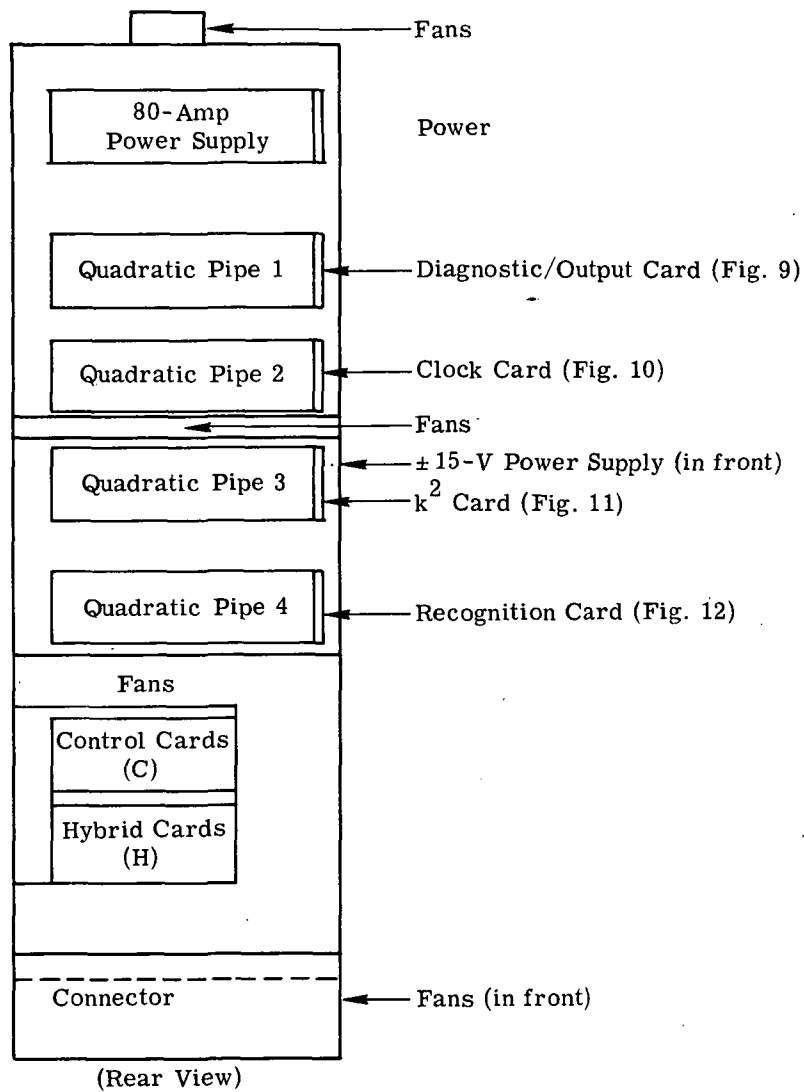


FIGURE 2. LOCATION OF MAJOR MIDAS COMPONENTS

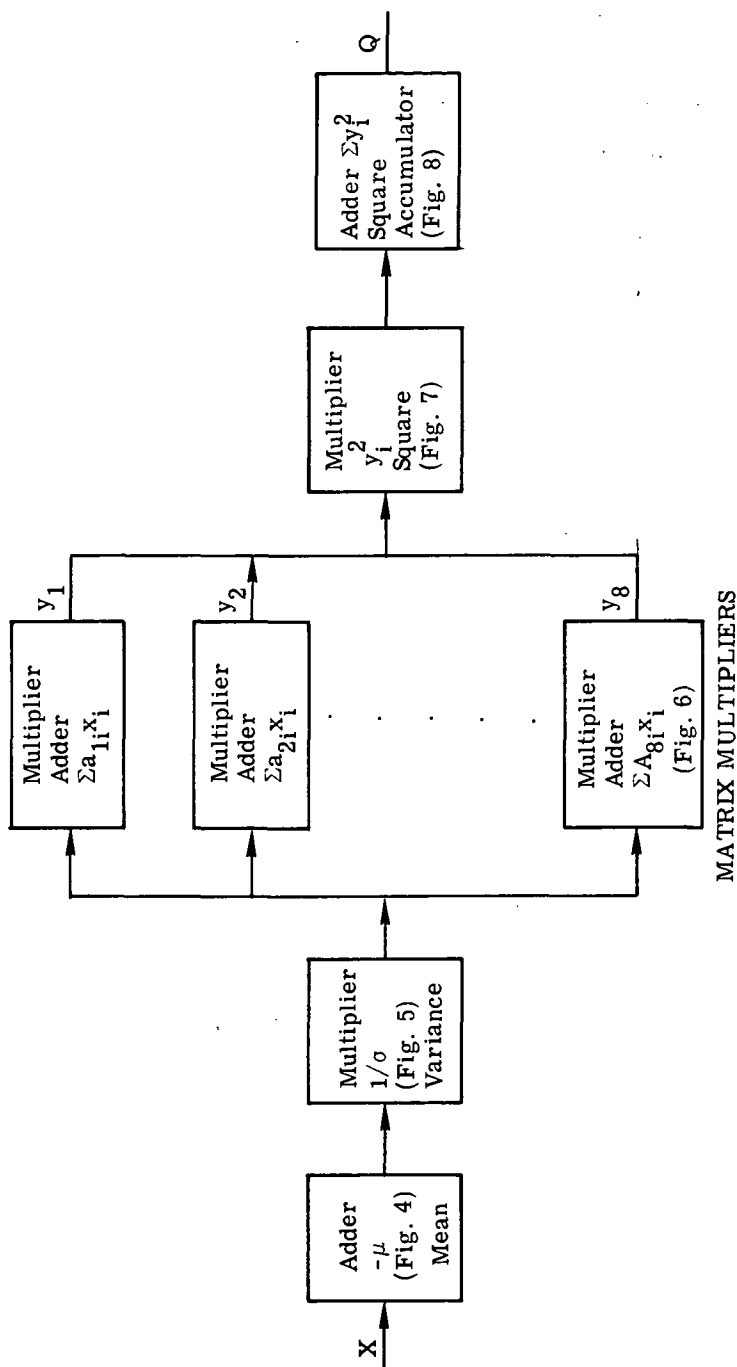


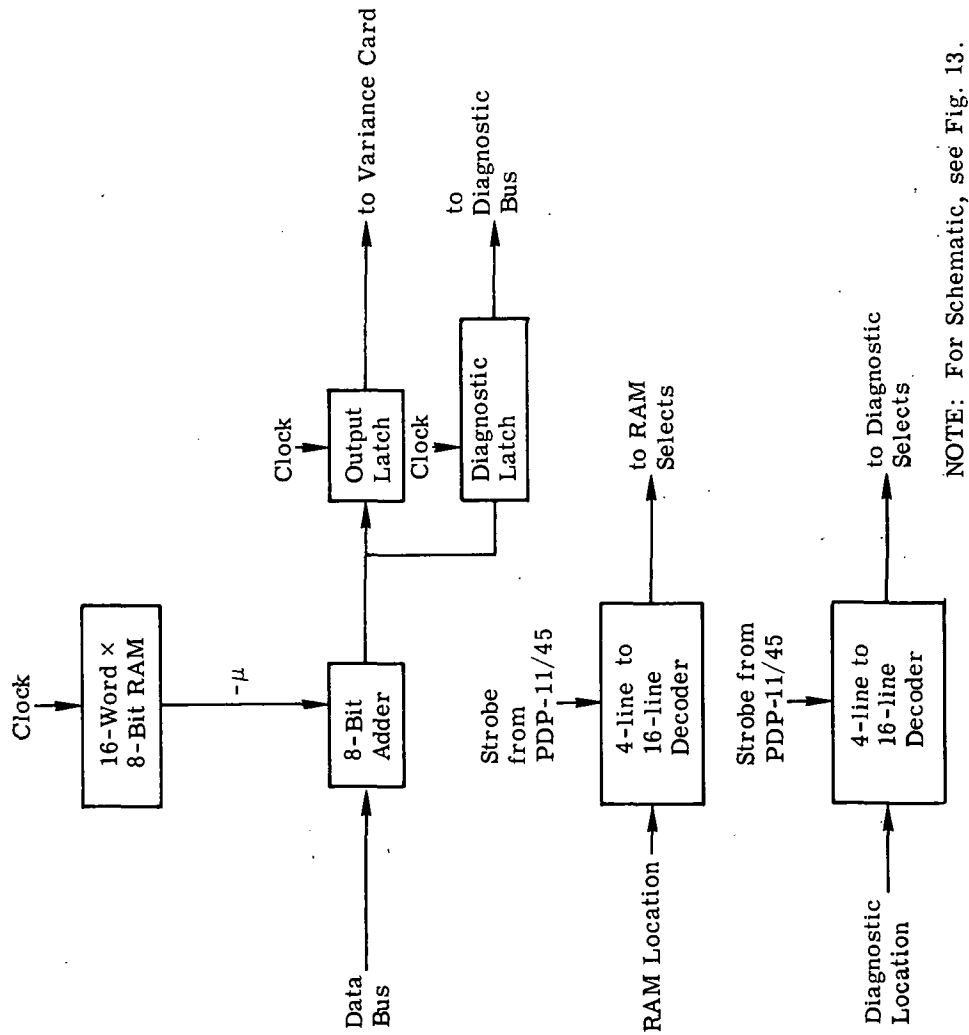
FIGURE 3. BLOCK DIAGRAM OF THE QUADRATIC PIPE

3

CLASSIFIER SECTION

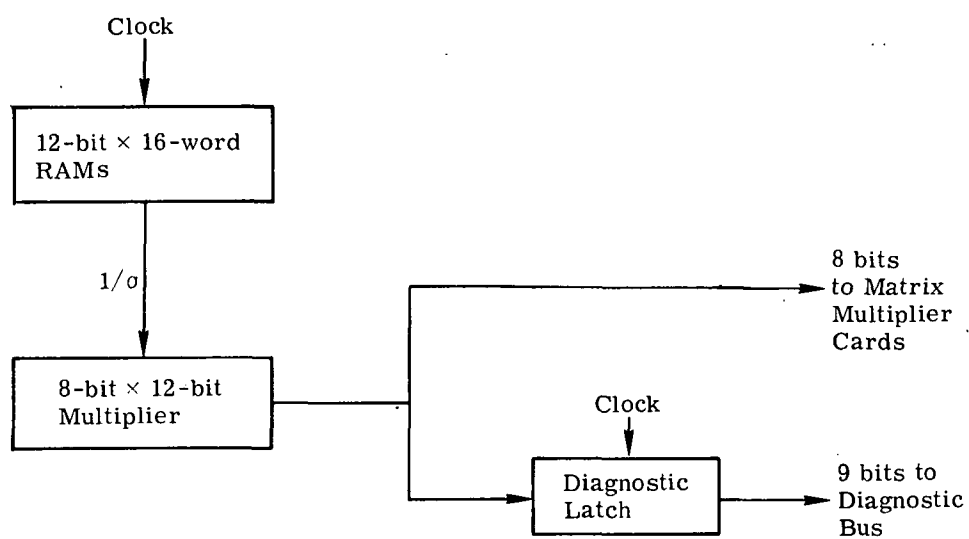
A detailed description of the Classifier is given in Sections 4 and 6 of Volume I.

A block diagram of the quadratic pipe computation is shown in Fig. 3.



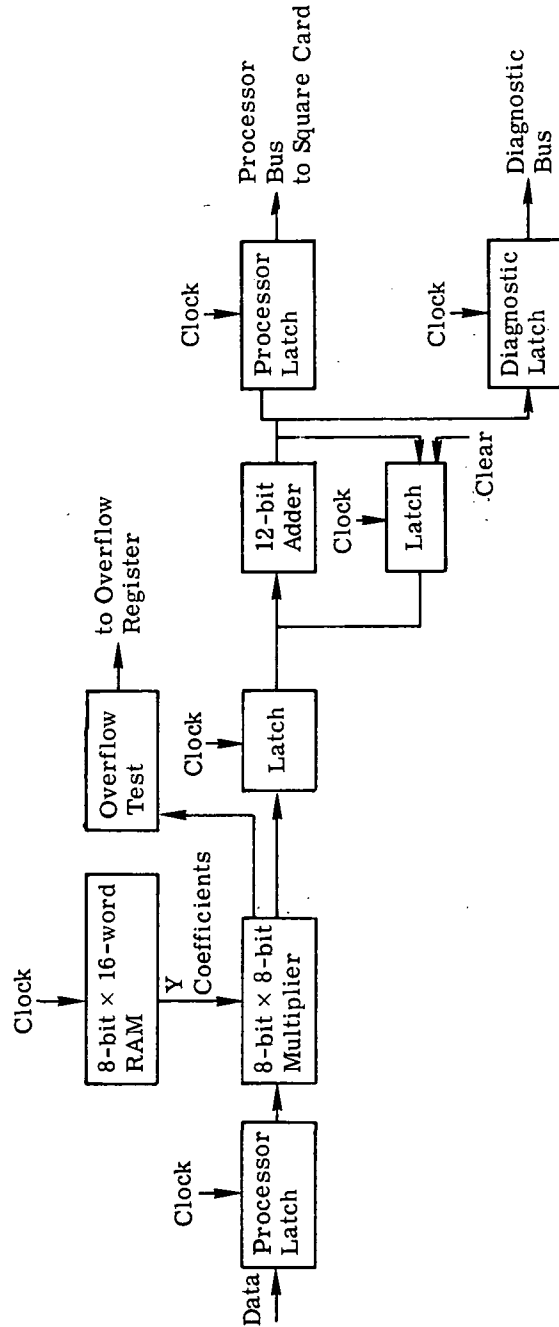
NOTE: For Schematic, see Fig. 13.

FIGURE 4. BLOCK DIAGRAM OF THE MEAN CARD



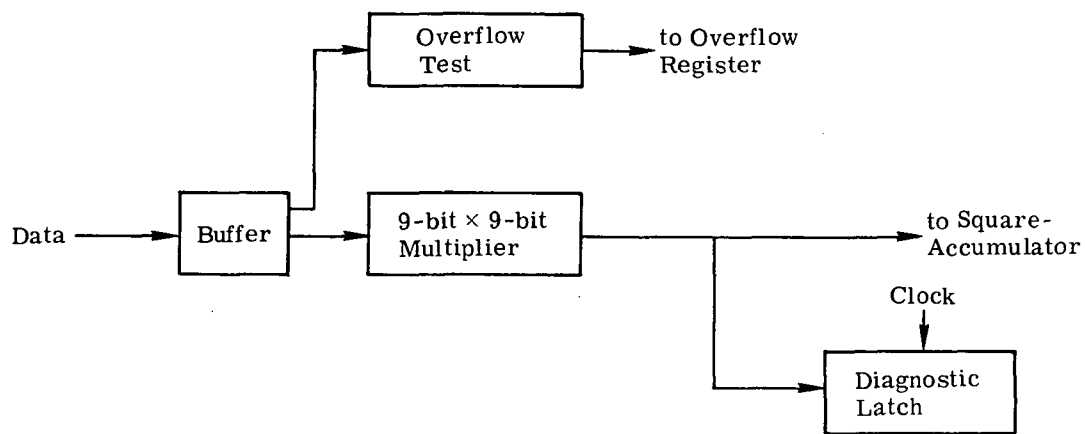
NOTE: For Schematic, see Fig. 14.

FIGURE 5. BLOCK DIAGRAM OF THE VARIANCE CARD



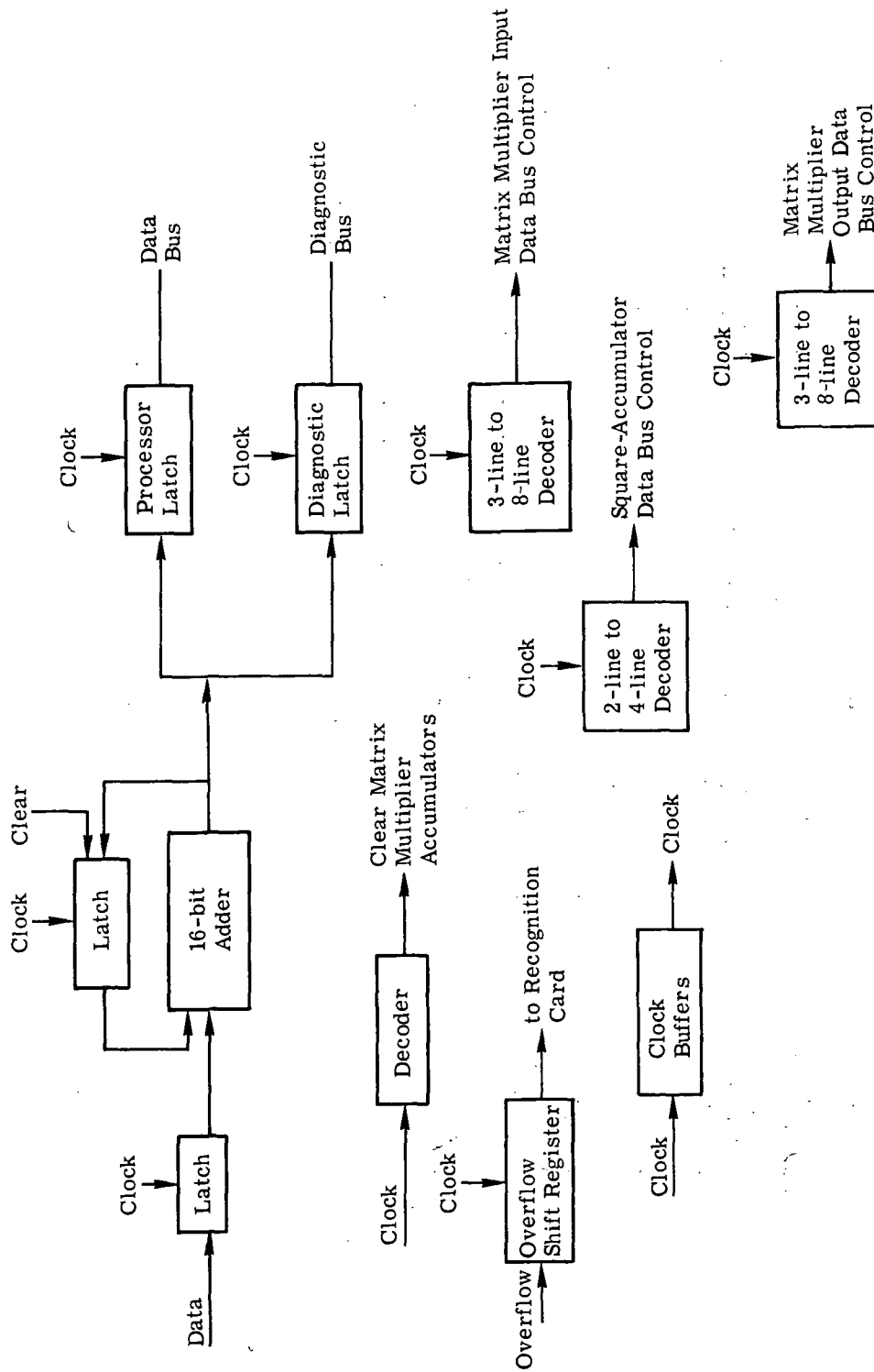
NOTE: For Schematic, see Fig. 15.

FIGURE 6. BLOCK DIAGRAM OF THE MATRIX MULTIPLIER CARD



NOTE: For Schematic, see Fig. 16.

FIGURE 7. BLOCK DIAGRAM OF THE SQUARE CARD



NOTE: For Schematic, see Figure 17.

FIGURE 8. BLOCK DIAGRAM OF THE SQUARE-ACCUMULATOR CARD

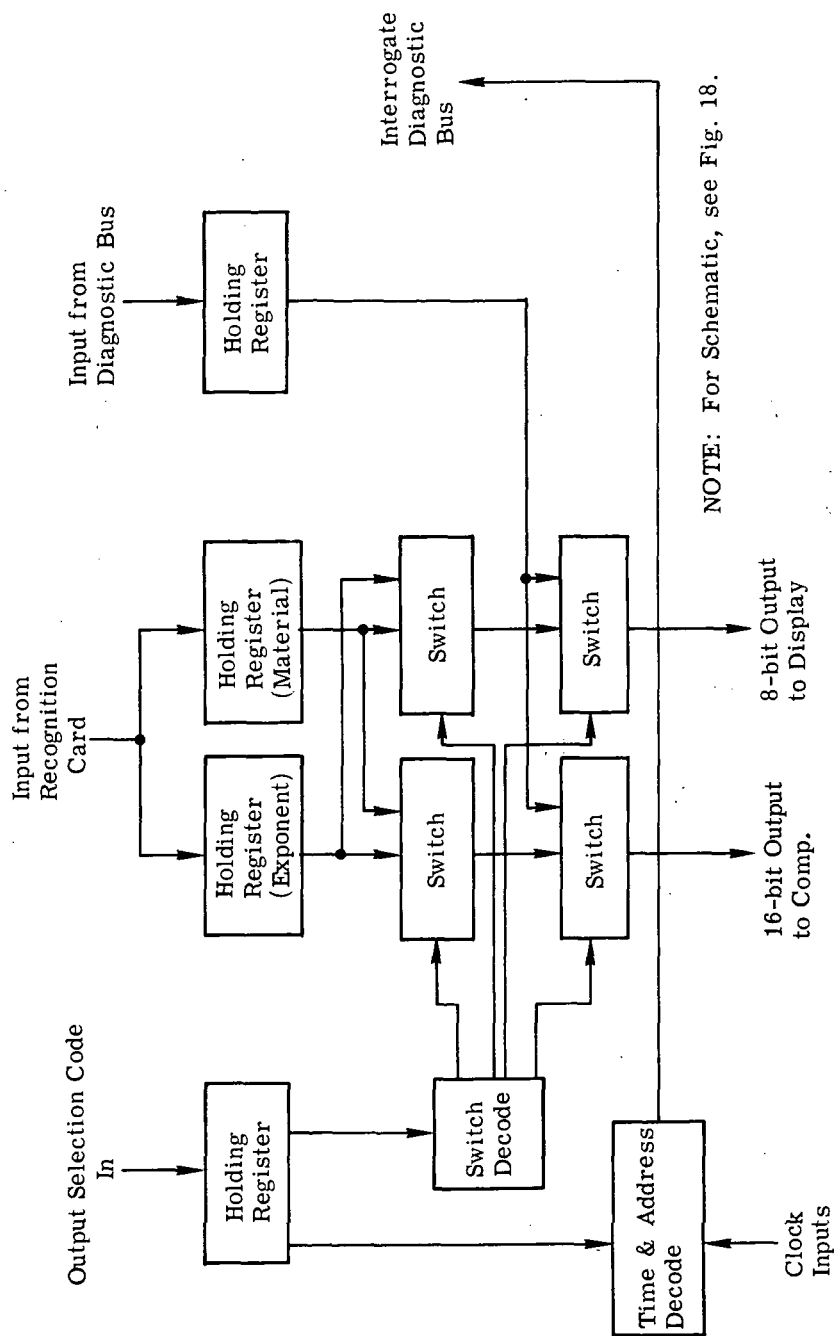
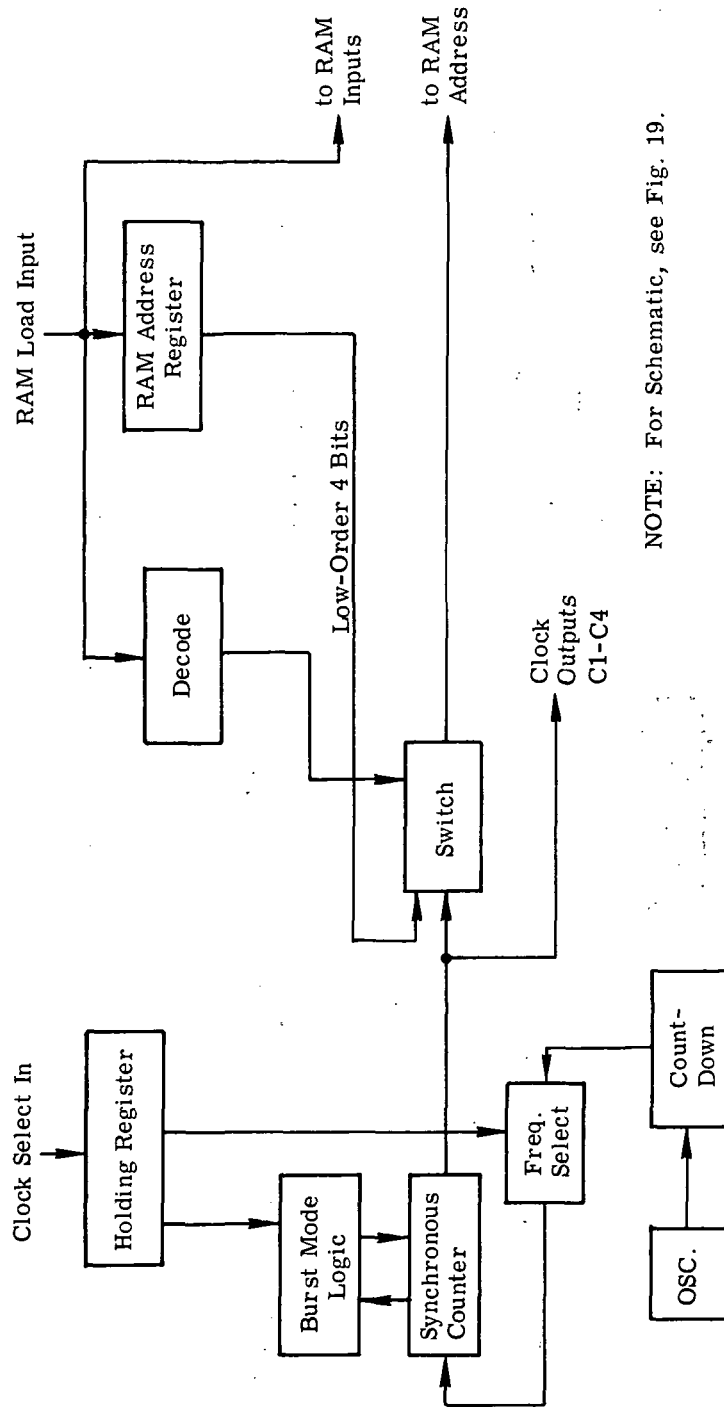
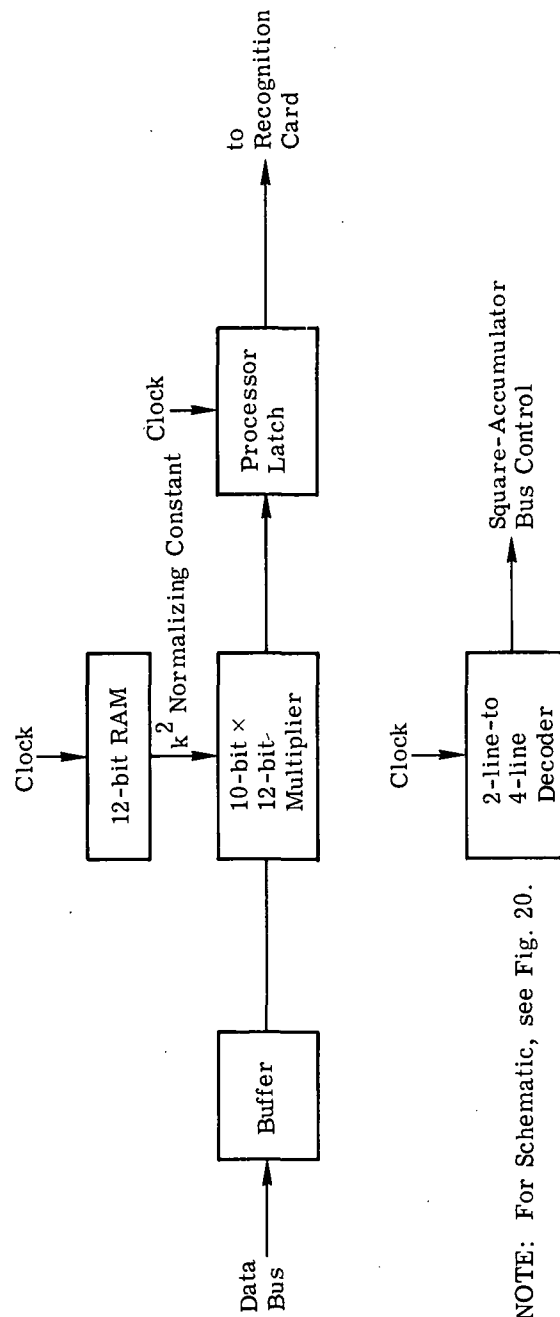


FIGURE 9. BLOCK DIAGRAM OF THE DIAGNOSTIC/OUTPUT CARD



NOTE: For Schematic, see Fig. 19.

FIGURE 10. BLOCK DIAGRAM OF THE CLOCK CARD



NOTE: For Schematic, see Fig. 20.

FIGURE 11. BLOCK DIAGRAM OF THE k^2 CARD

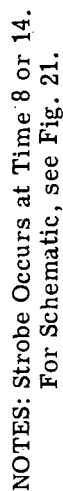
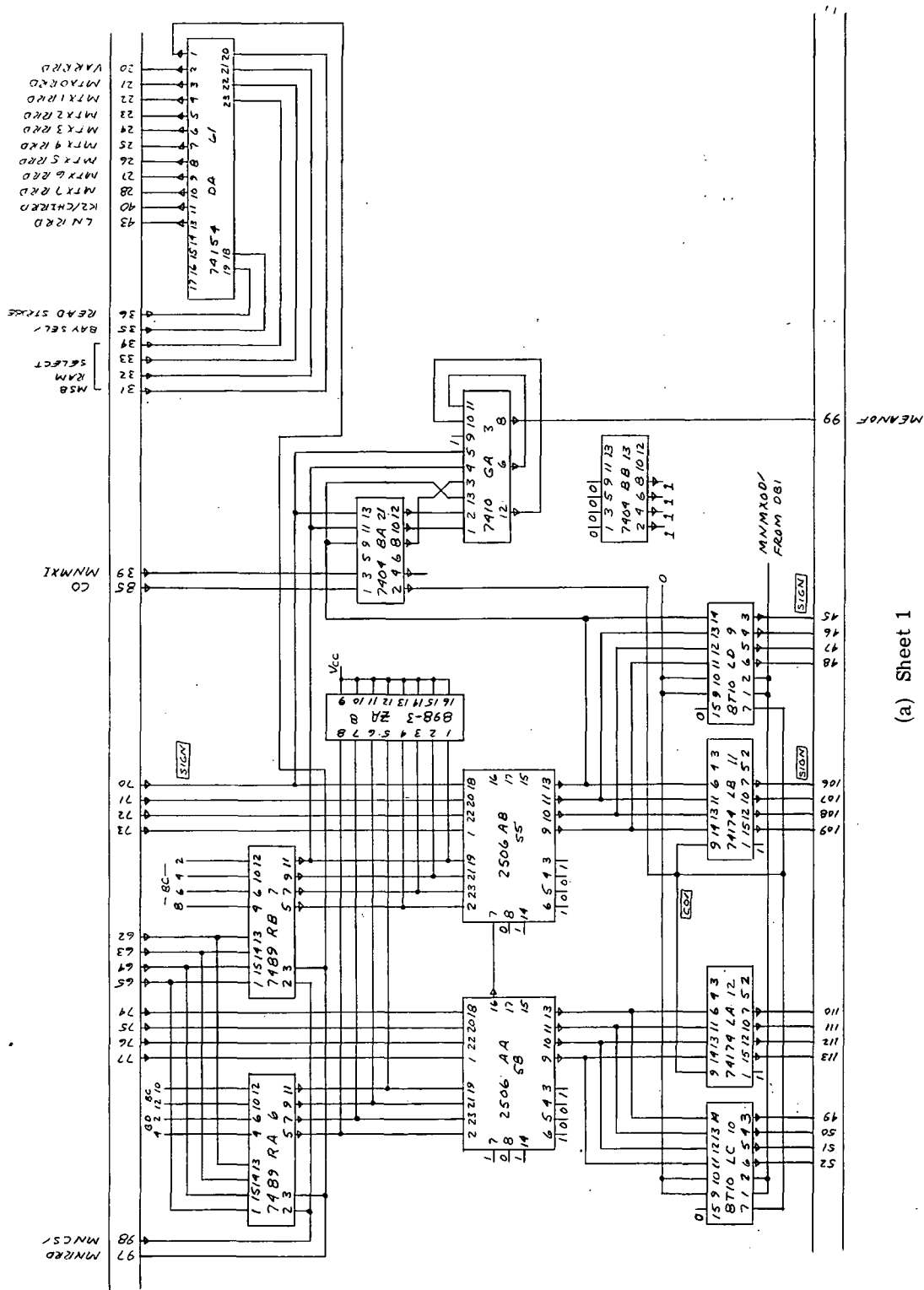
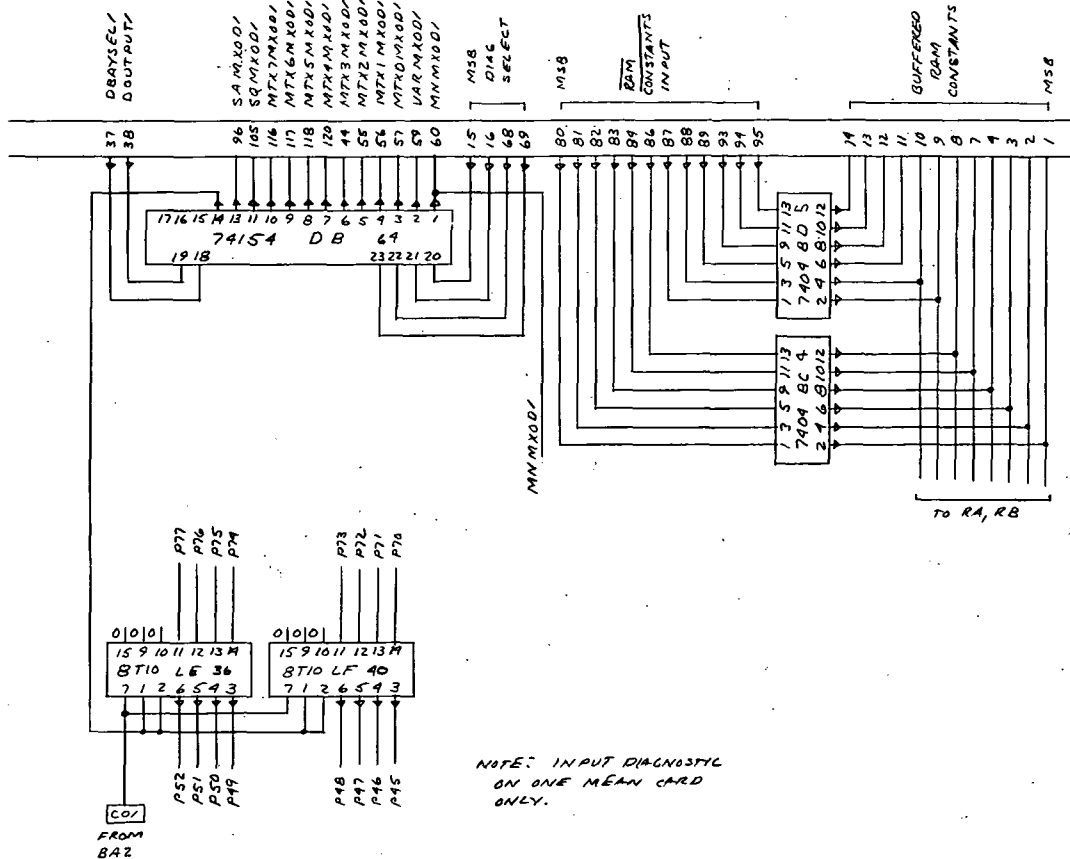


FIGURE 12. BLOCK DIAGRAM OF THE RECOGNITION CARD



(a) Sheet 1

FIGURE 13. MEAN (MN) (Continued)



(b) Sheet 2

FIGURE 13. MEAN (MN) (Concluded)

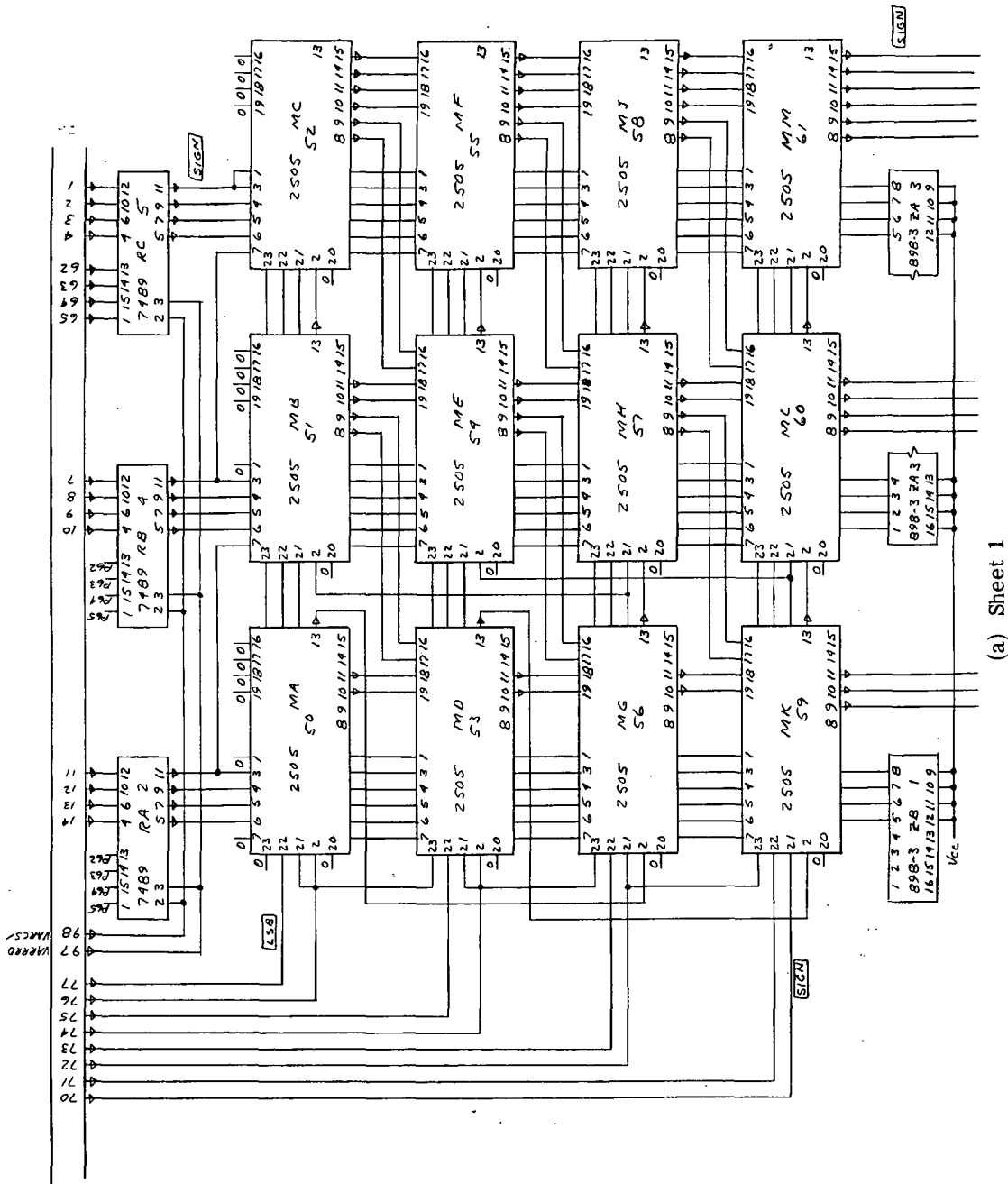


FIGURE 15. VARIANCE (VAR) (Continued)

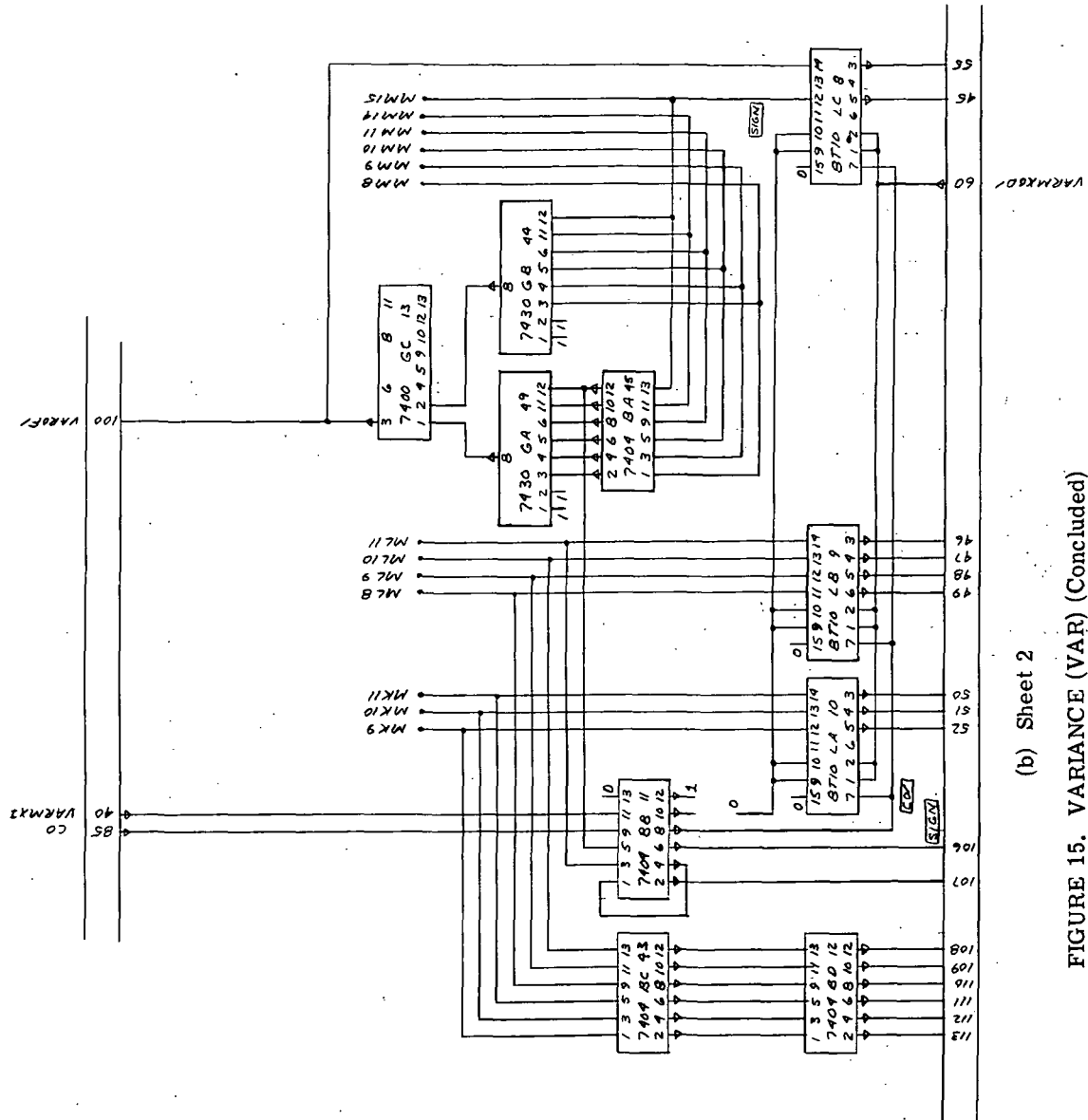


FIGURE 15. VARIANCE (VAR) (Concluded)

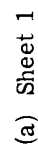
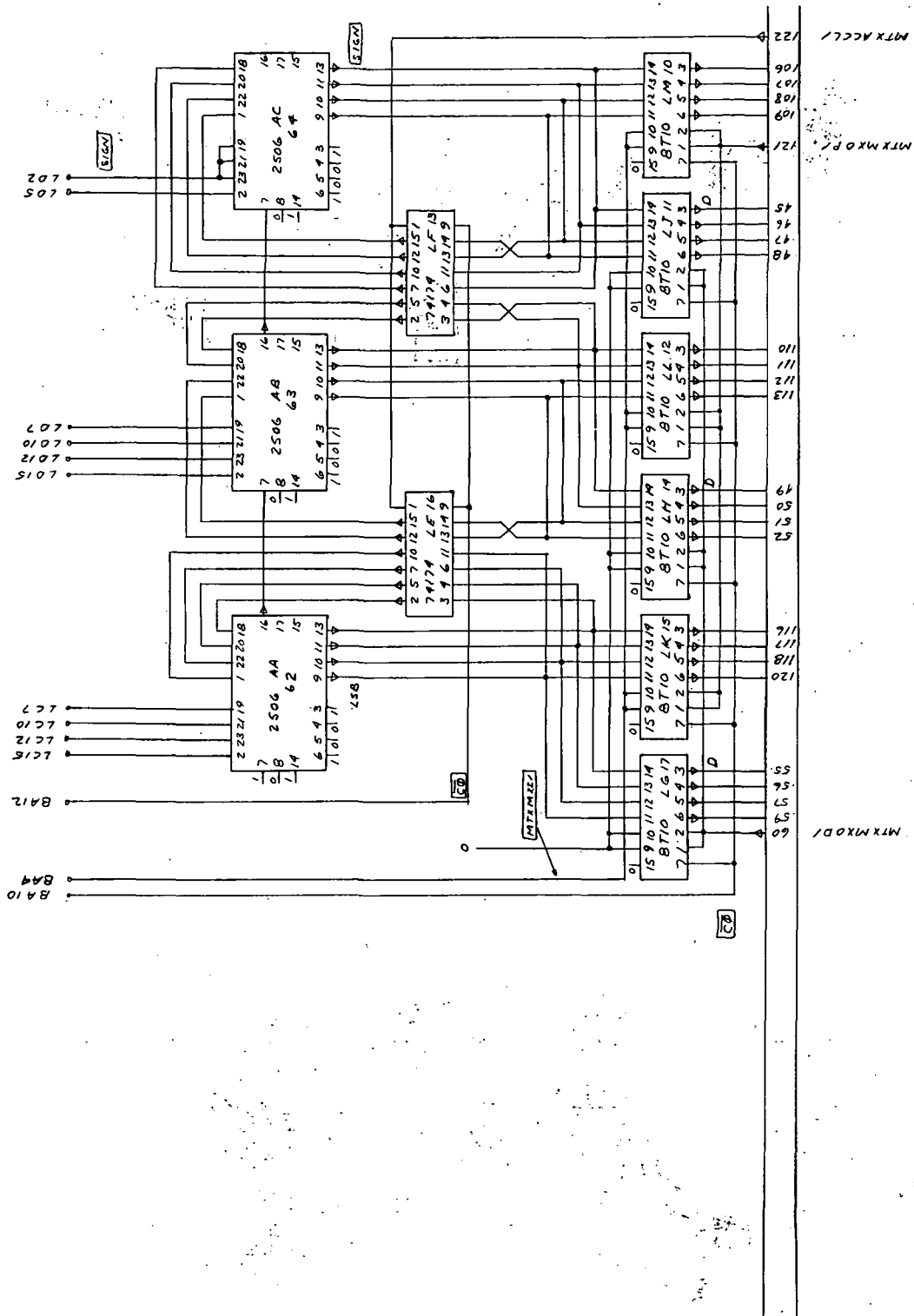
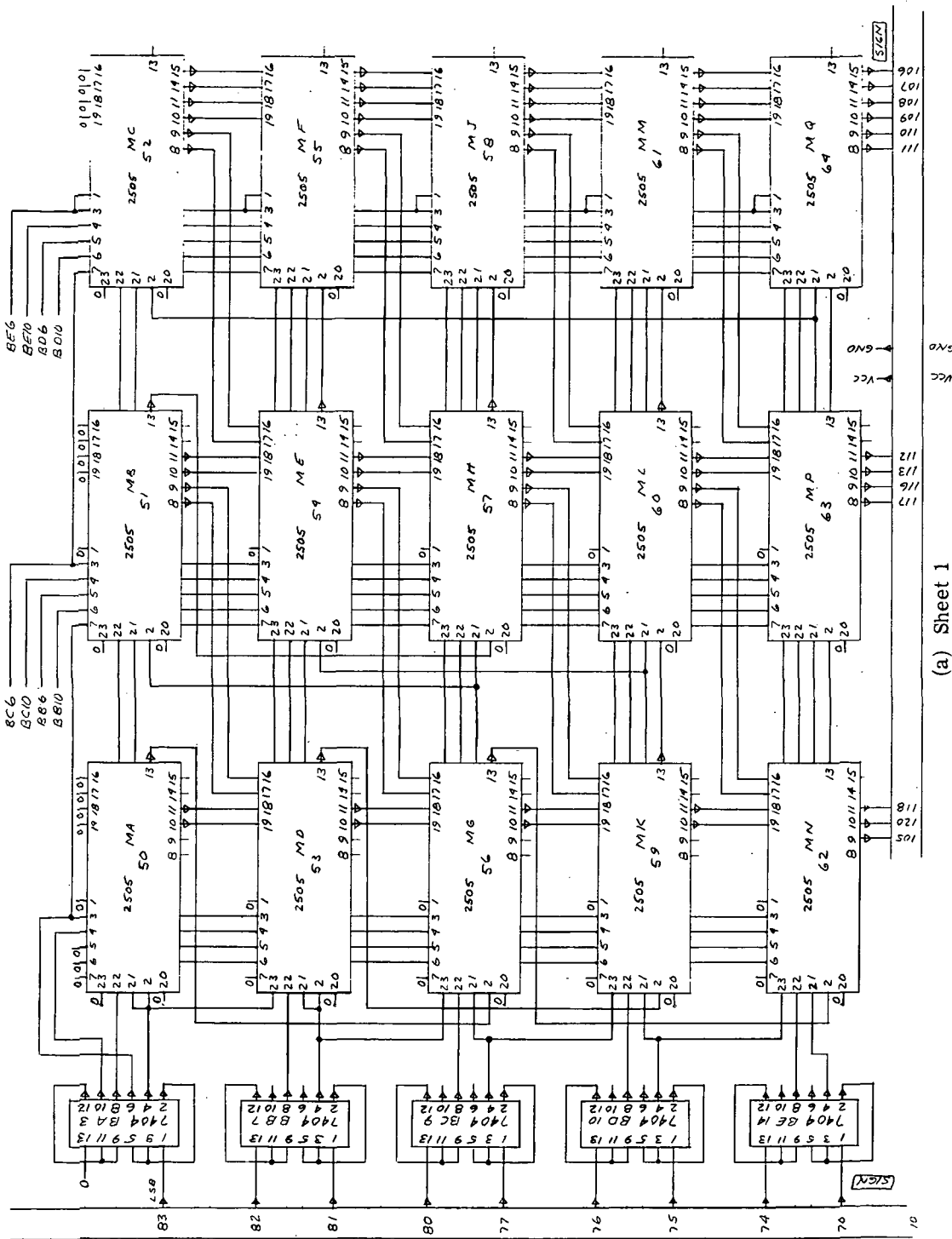


FIGURE 15. 8×8 MATRIX MULTIPLIER (MTX) (Continued)



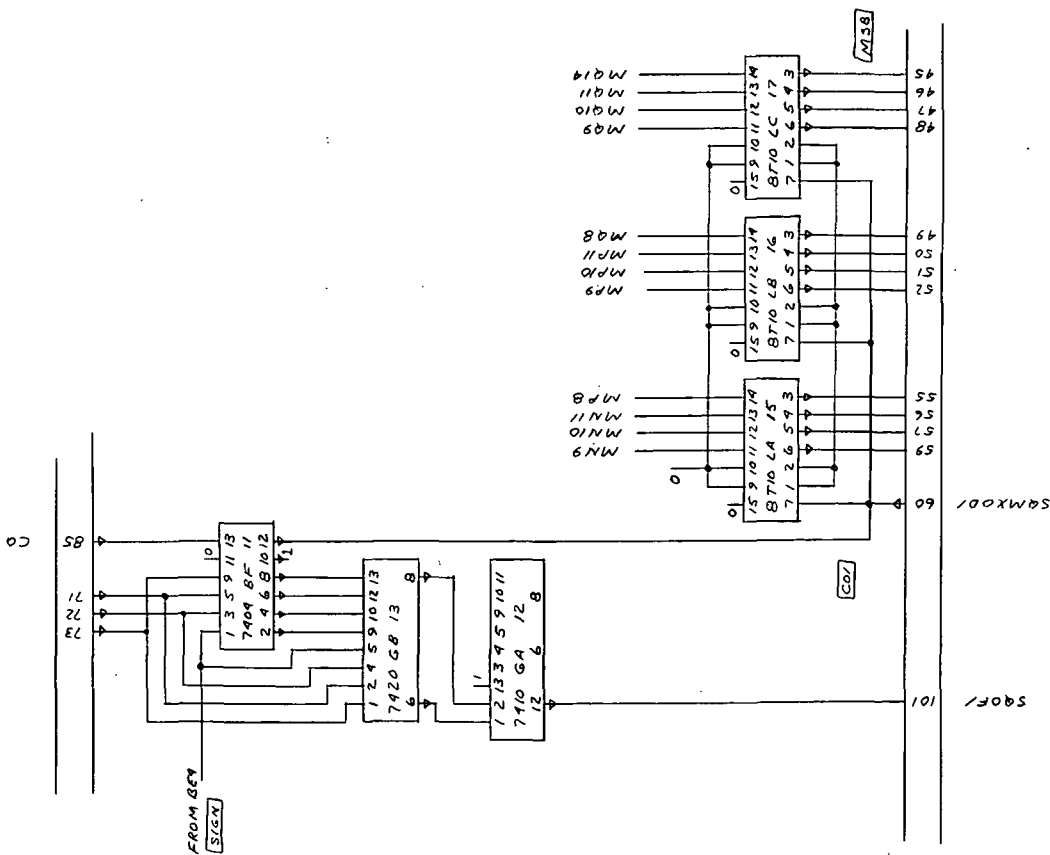
(b) Sheet 2

FIGURE 15. 8 x 8 MATRIX MULTIPLIER (MTX) (Concluded)

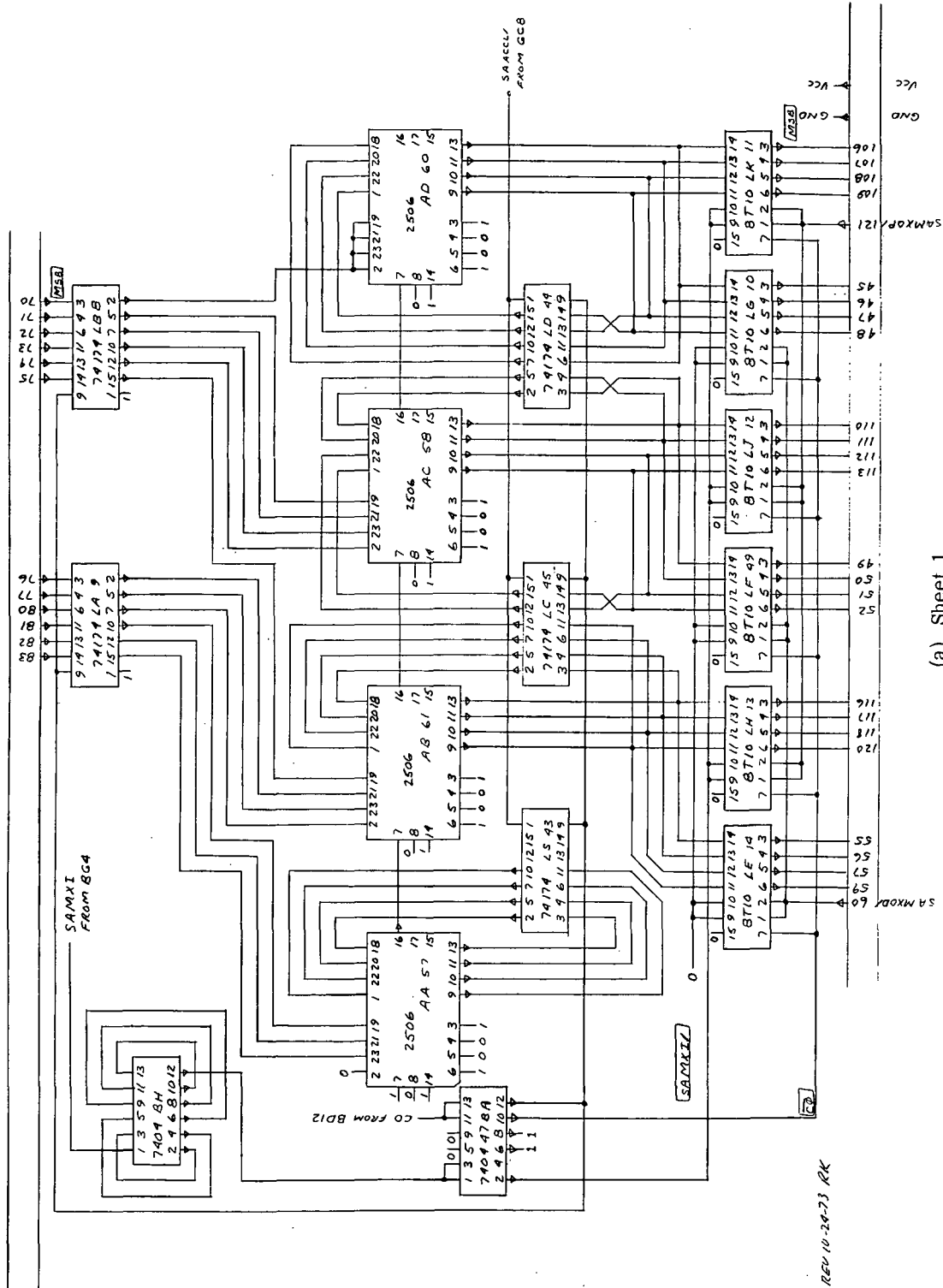


(a) Sheet 1

FIGURE 16. 9 x 9 SQUARE CARD (SQ) (Continued)



(b) Sheet 2
FIGURE 16. 9 x 9 SQUARE CARD (SQ) (Concluded)



(a) Sheet 1
FIGURE 17. SQUARE-ACCUMULATOR (SA) (Continued)

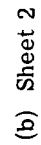


FIGURE 17. SQUARE-ACCUMULATOR (SA) (Concluded)

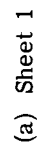


FIGURE 18. DIAGNOSTIC/OUTPUT (Continued)

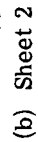


FIGURE 18. DIAGNOSTIC/OUTPUT (Continued)

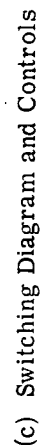


FIGURE 18. DIAGNOSTIC/OUTPUT (Concluded)

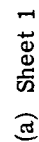
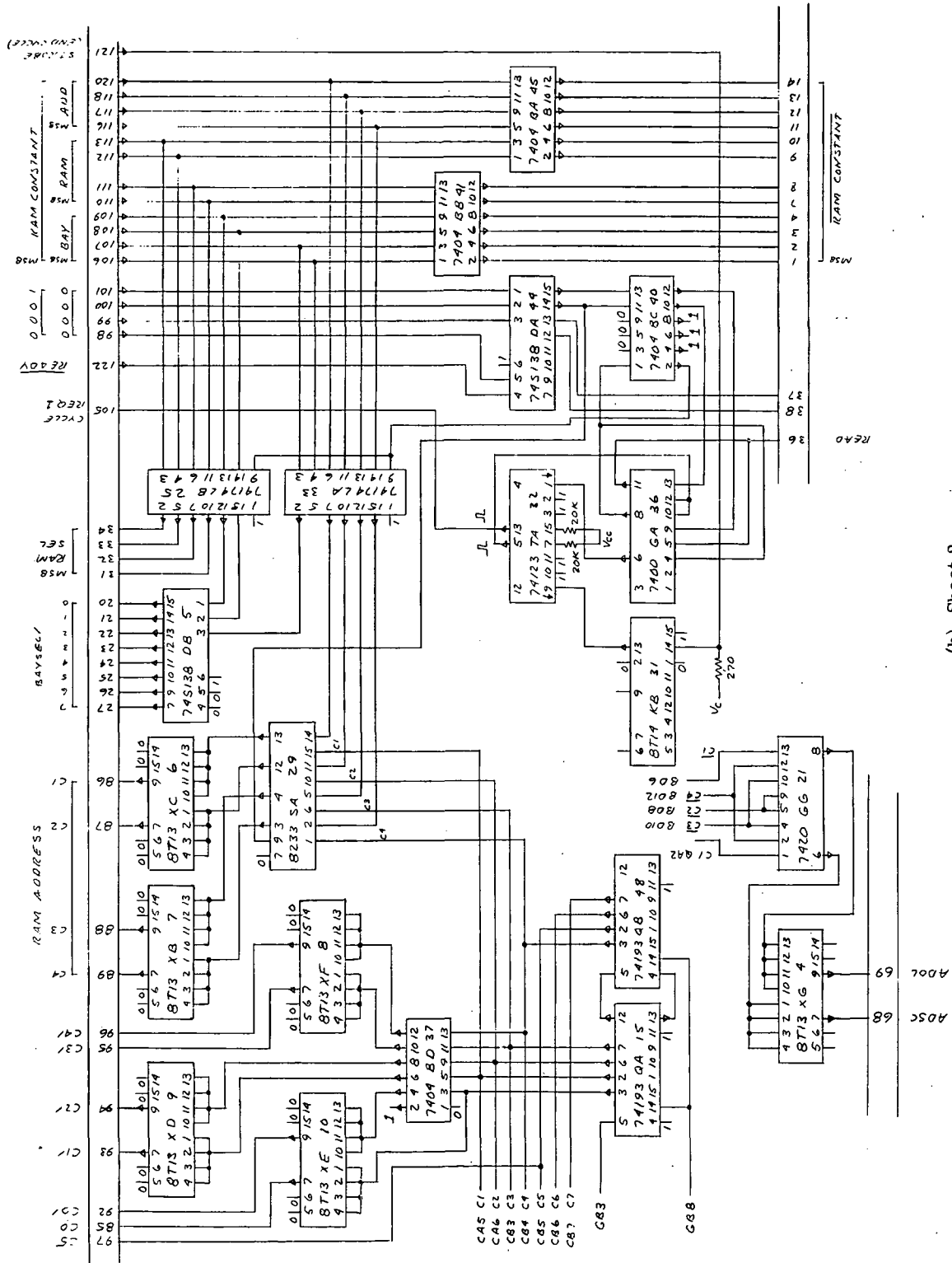
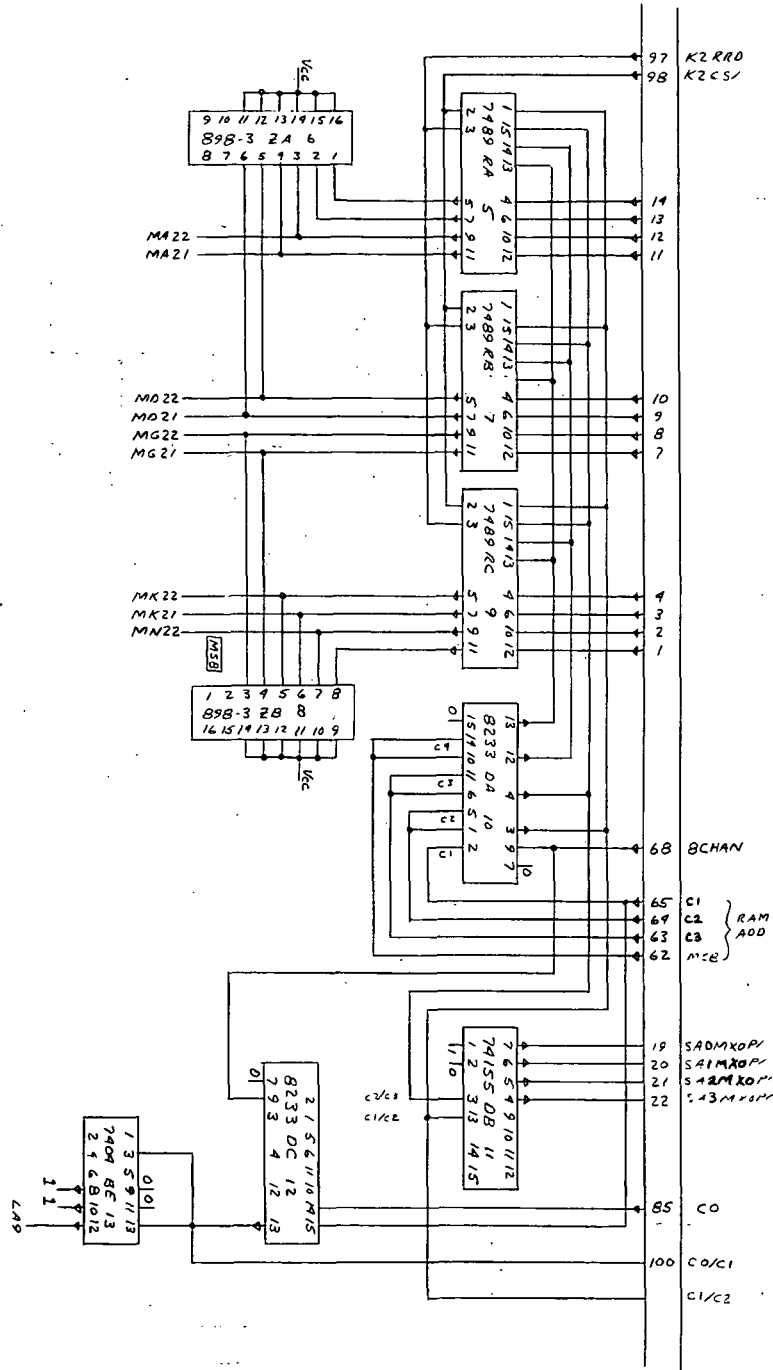


FIGURE 19. CLOCK (Continued)



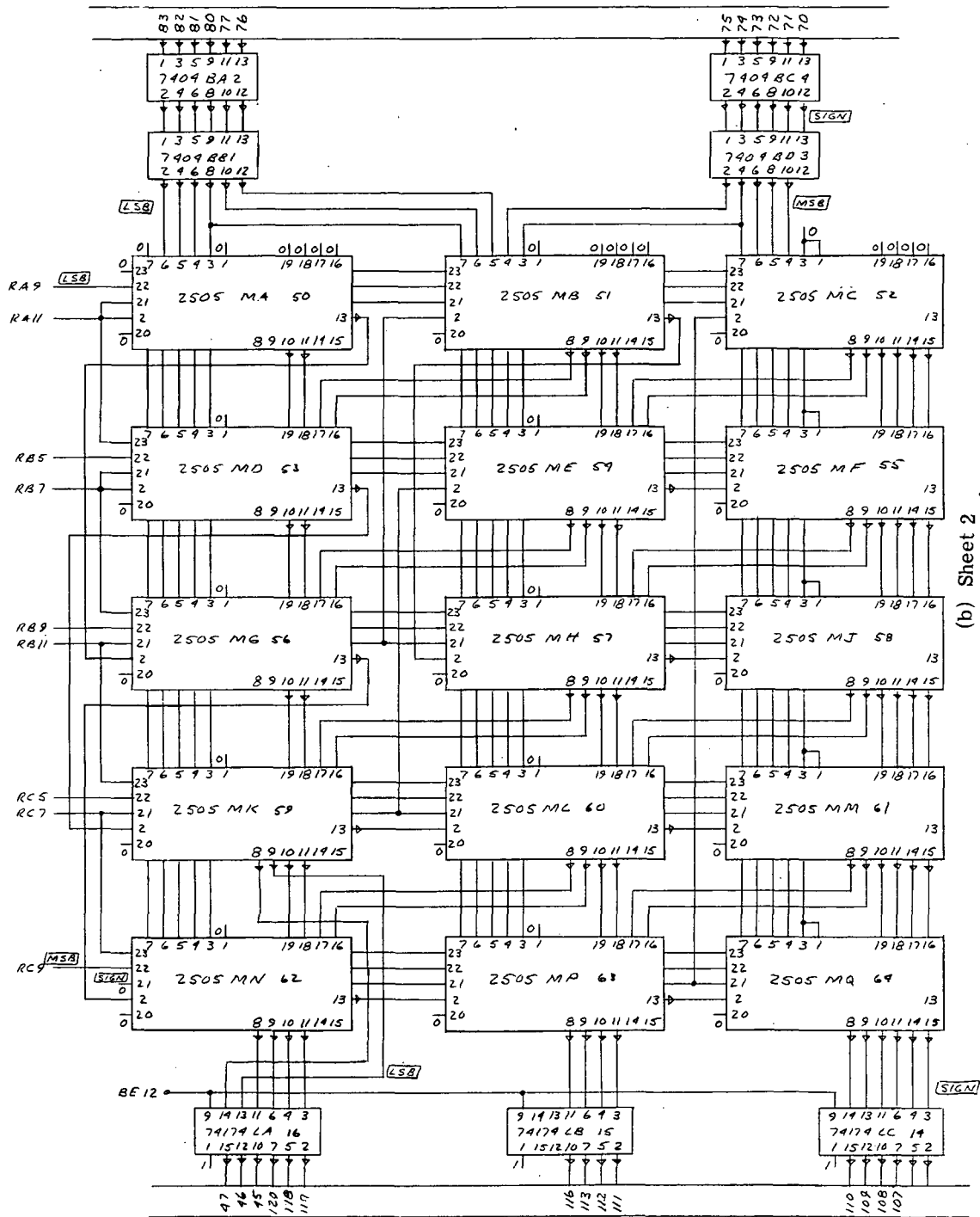
(b) Sheet 2

FIGURE 19. CLOCK (Concluded)

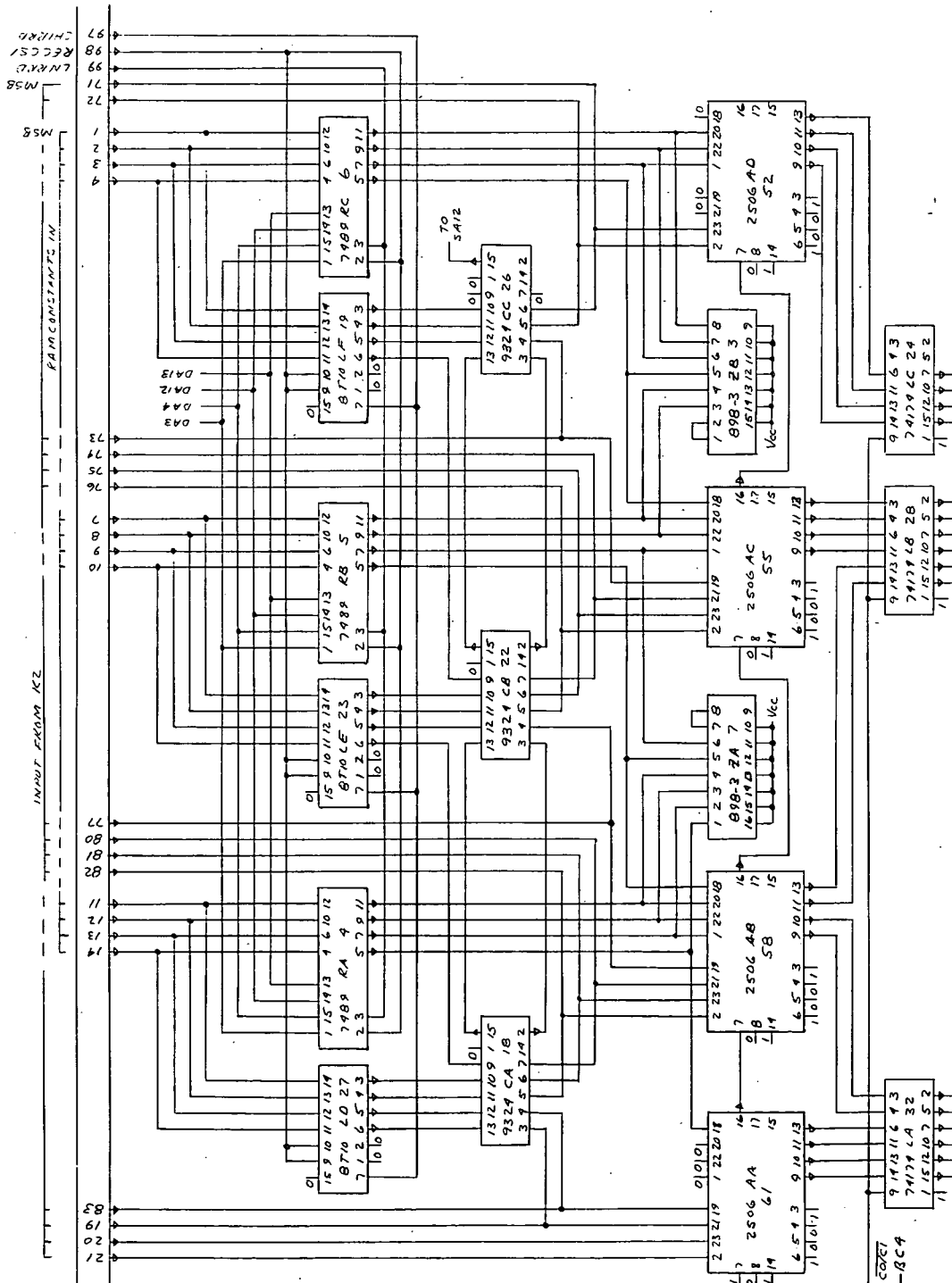


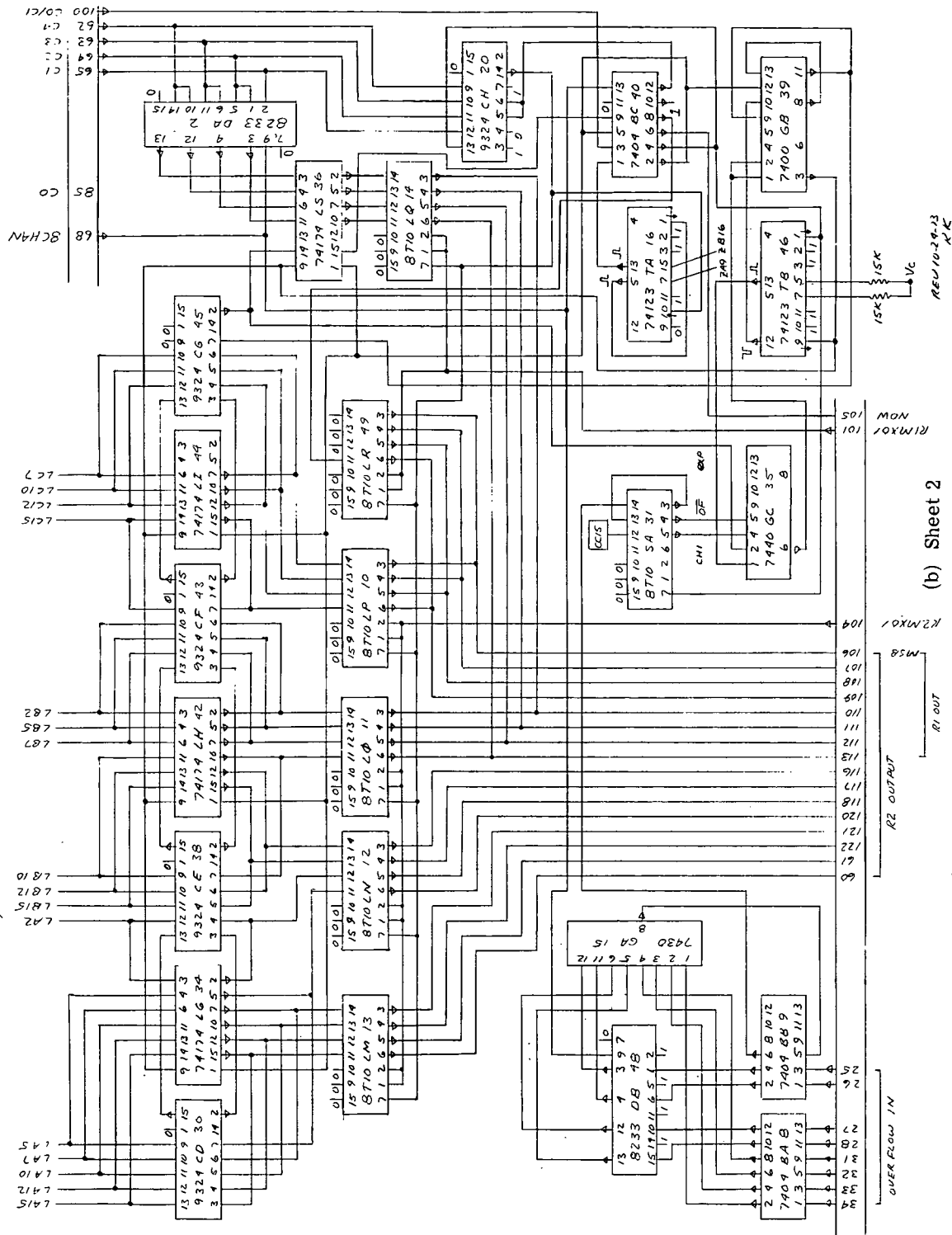
(a) Sheet 1,

FIGURE 20. k² (Continued)



(b) Sheet 2
FIGURE 20. k² (Concluded)





CONTROL AND HYBRID SECTION

The hybrid section of the classifier contains nineteen cards, of which sixteen are identical printed circuit cards. These cards, located in slots H-1 through H-16, perform the transfer of data to the classifier. A block diagram of the control and hybrid section is shown in Fig. 22 and a detailed block diagram of the hybrid cards is shown in Fig. 23. For a description of this classifier section, see Section 6 of Vol. I.

The transfer of data from the PDP-11/45 computer is accomplished by the circuitry shown in the block diagram of Fig. 24. The transfer of digitized data to the computer is controlled by the digital output synchronizer shown in the block diagram of Fig. 25.

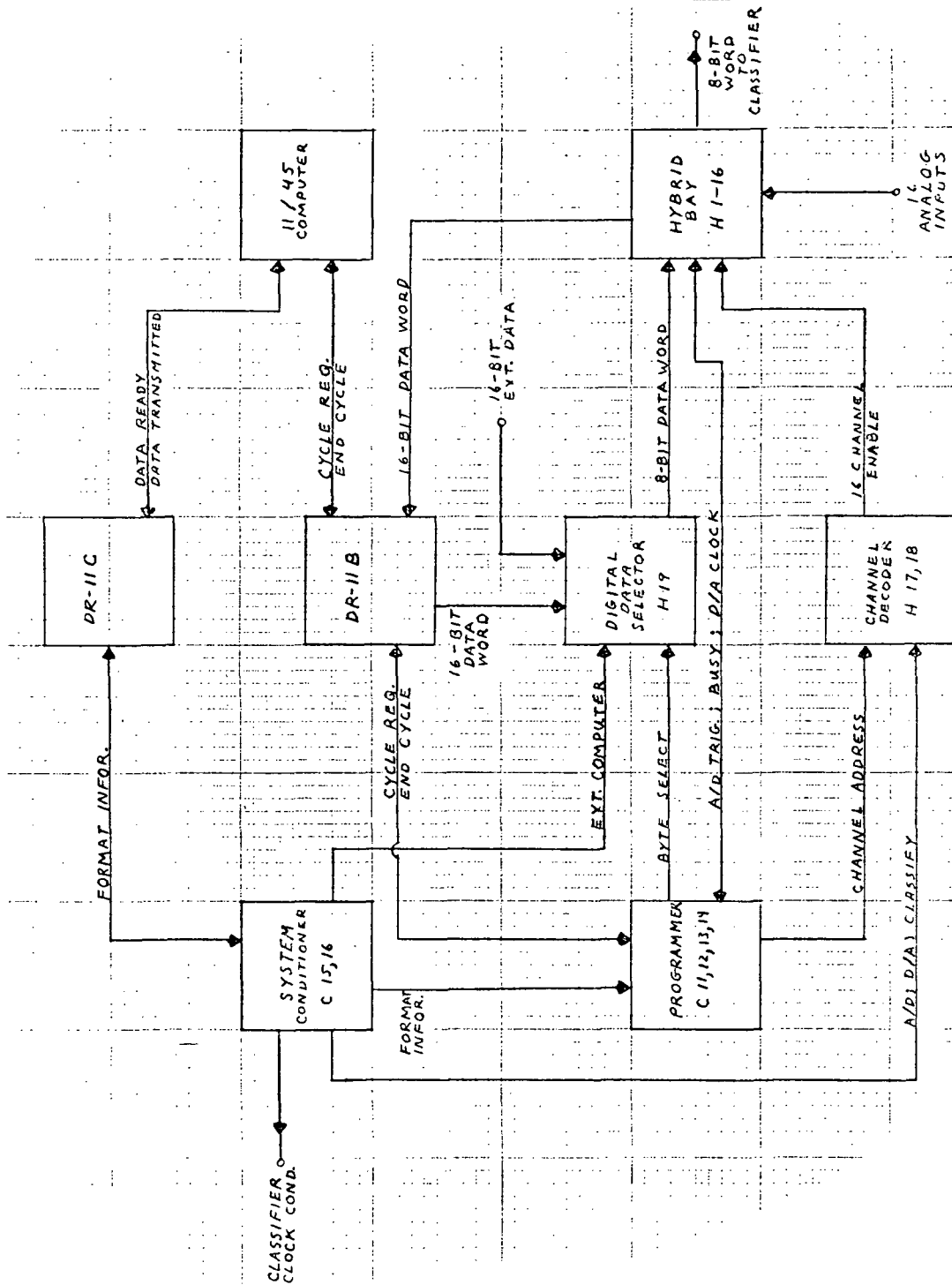


FIGURE 22. CONTROL SECTION

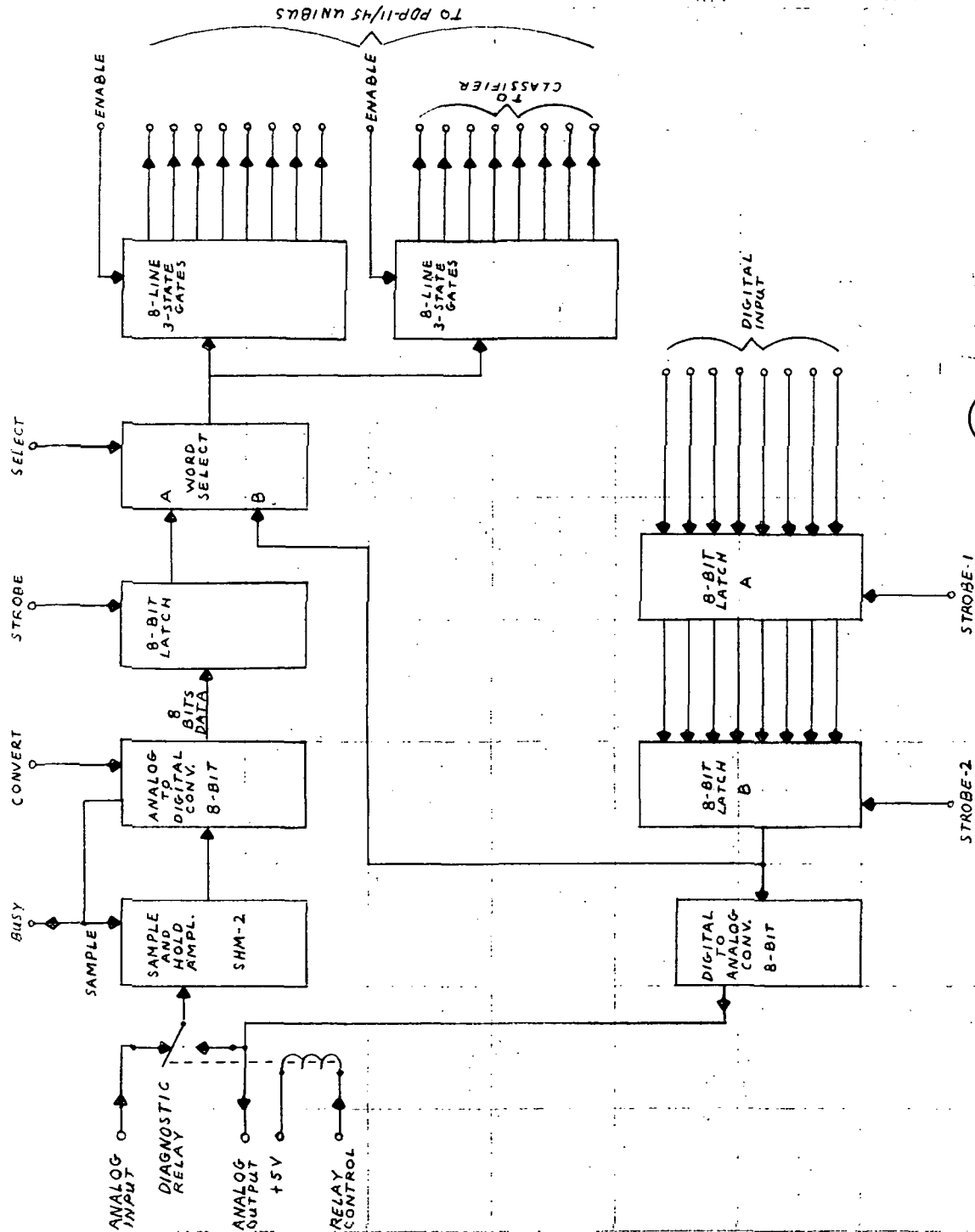


FIGURE 23. HYBRID BAY CARDS (H 1-16)

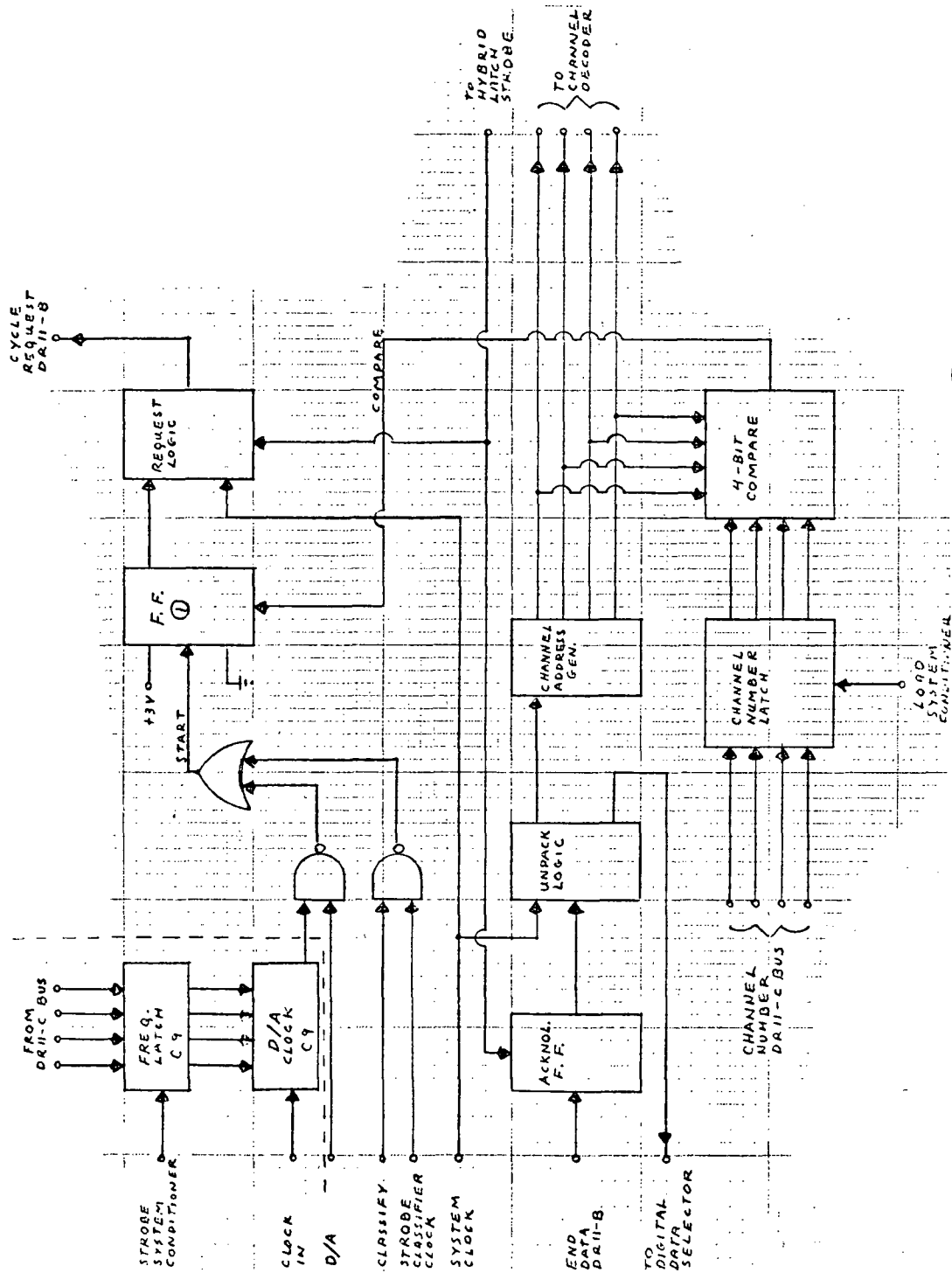
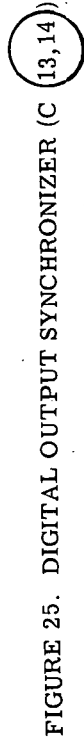


FIGURE 24. DIGITAL INPUT SYNCHRONIZER (C 11,12)



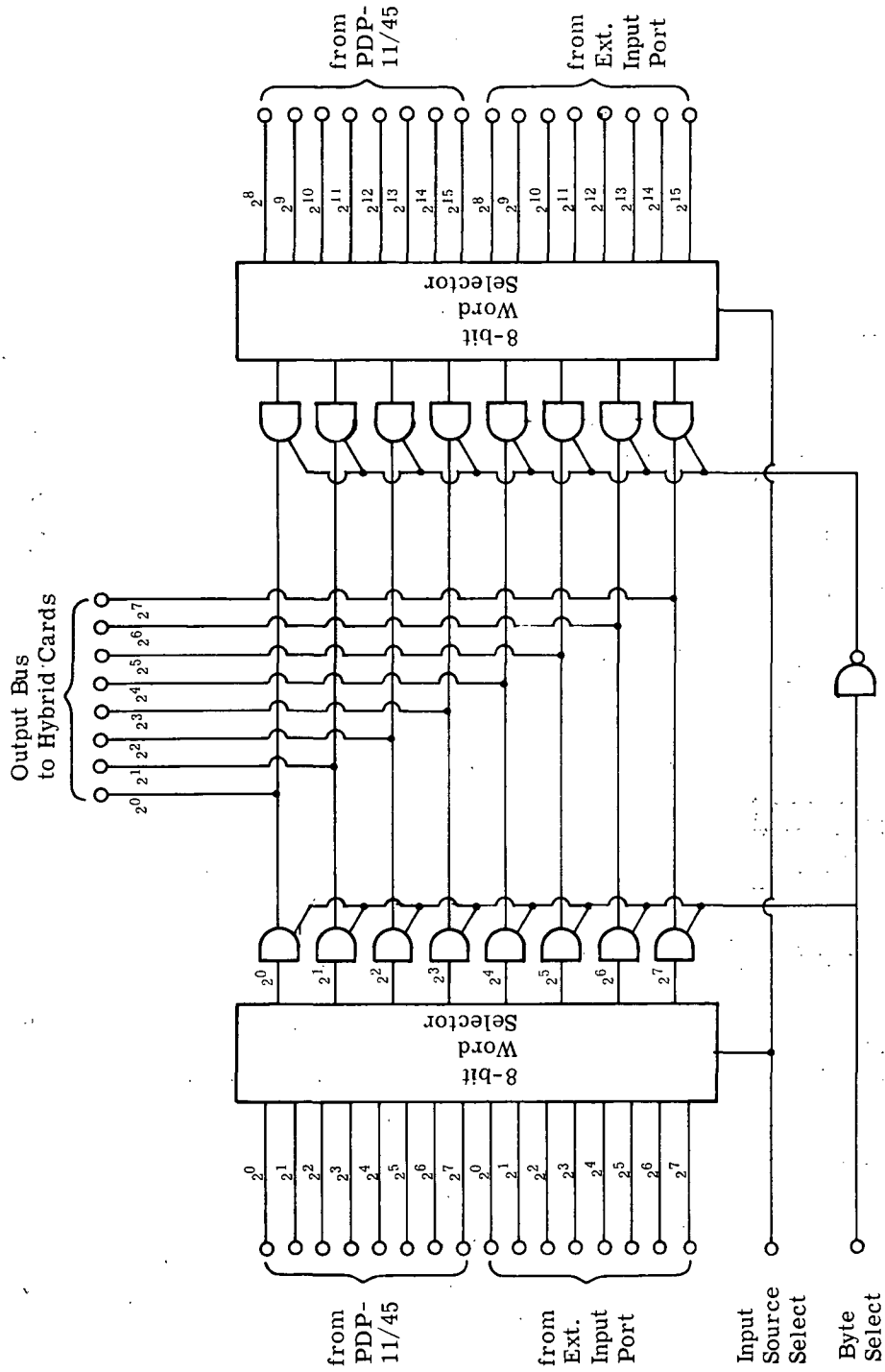


FIGURE 26. DIGITAL DATA SELECTOR (H 19)

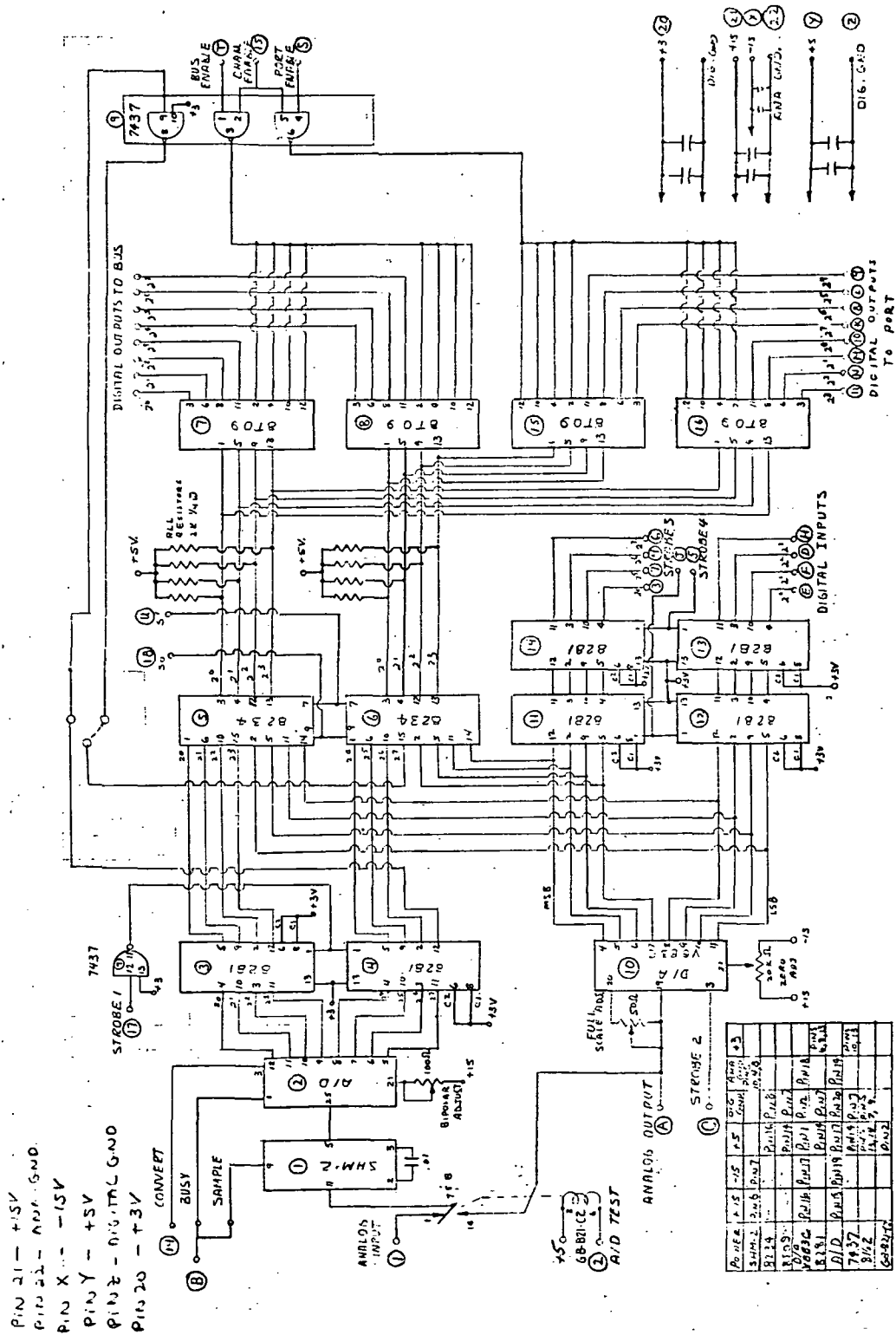


FIGURE 27. HYBRID CARDS (H 1-16)

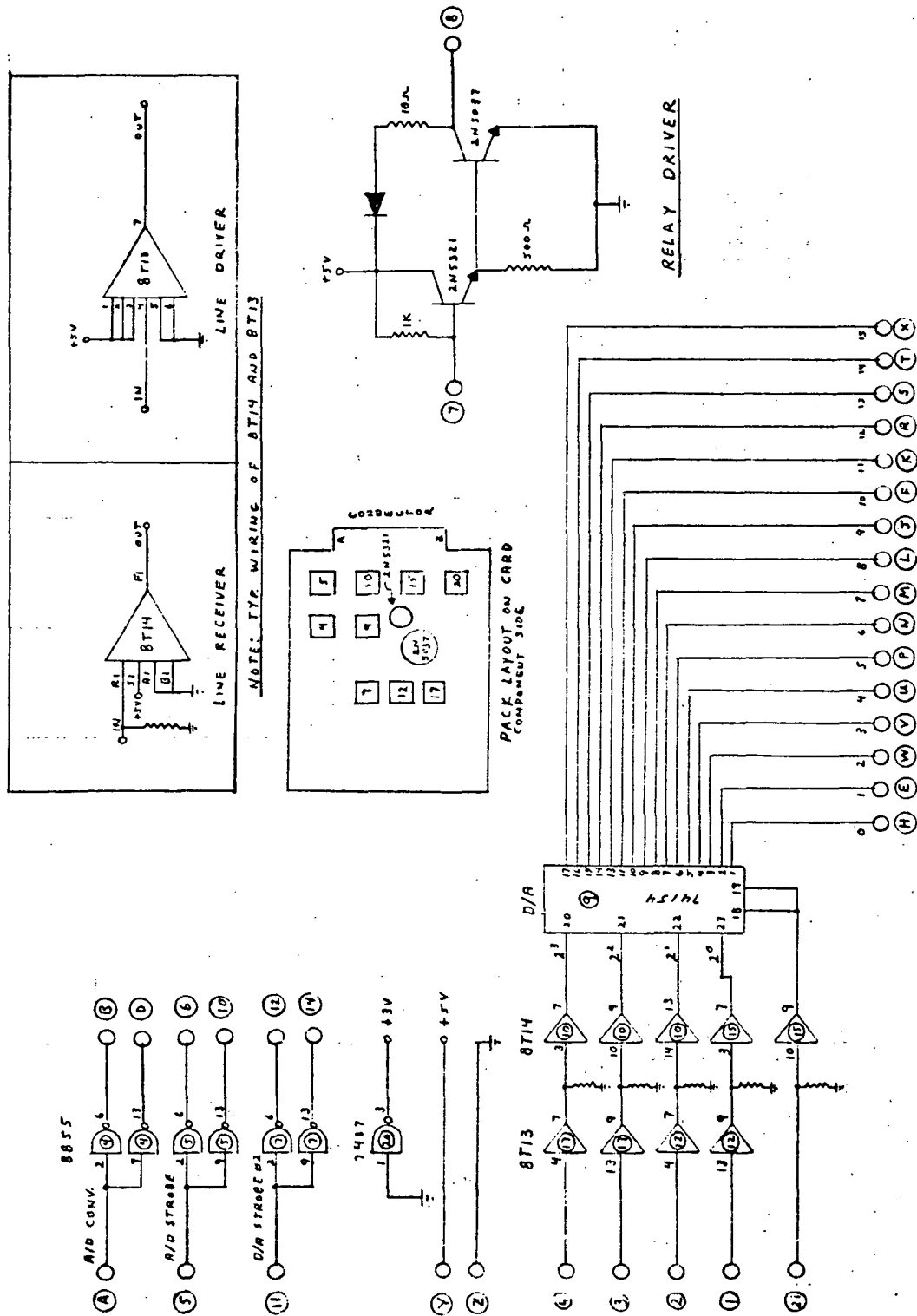


FIGURE 28. INPUT BUS AND PORT DECODER (H 17)

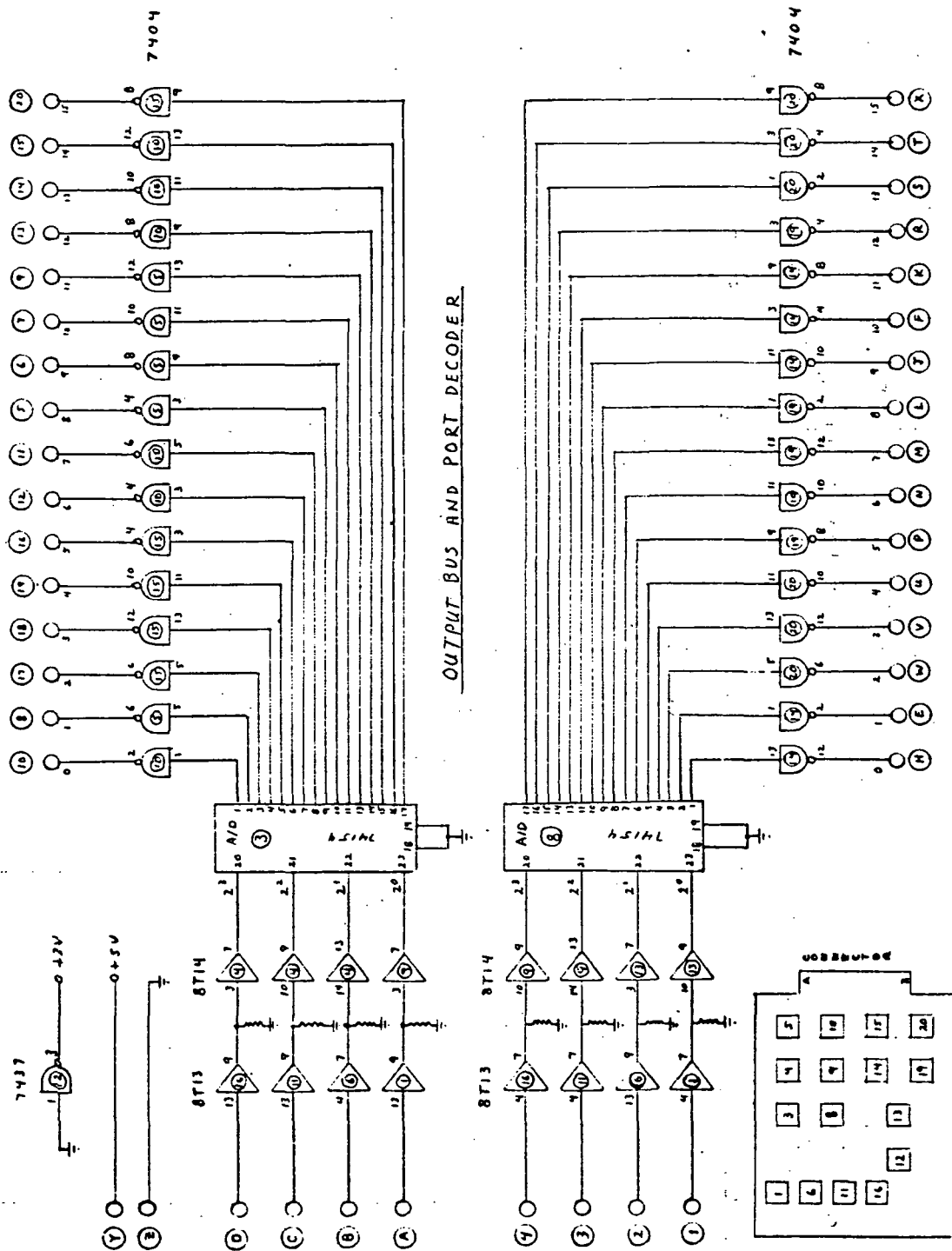


FIGURE 29. OUTPUT BUS AND PORT DECODER (H18)

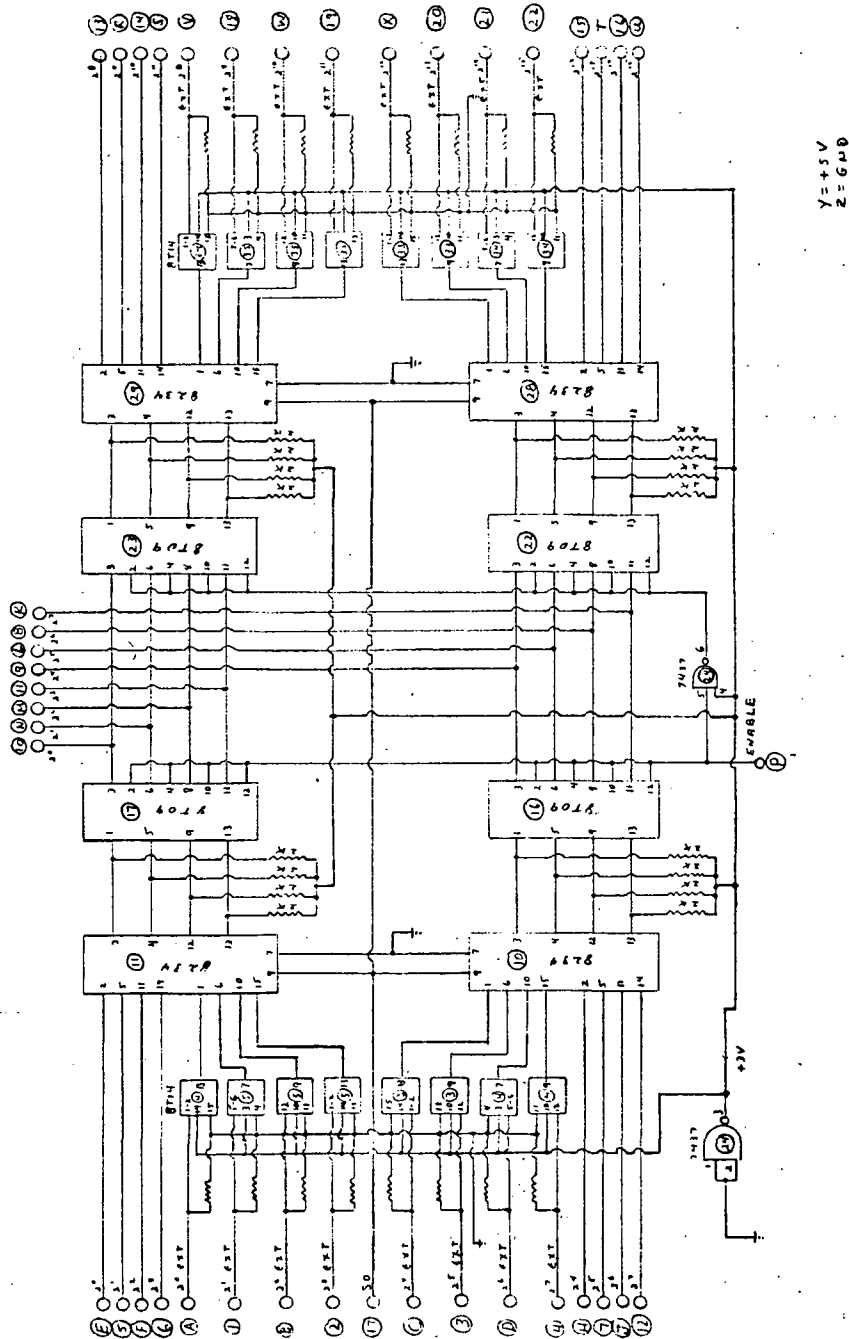


FIGURE 30. DIGITAL DATA SELECTOR (H 19)

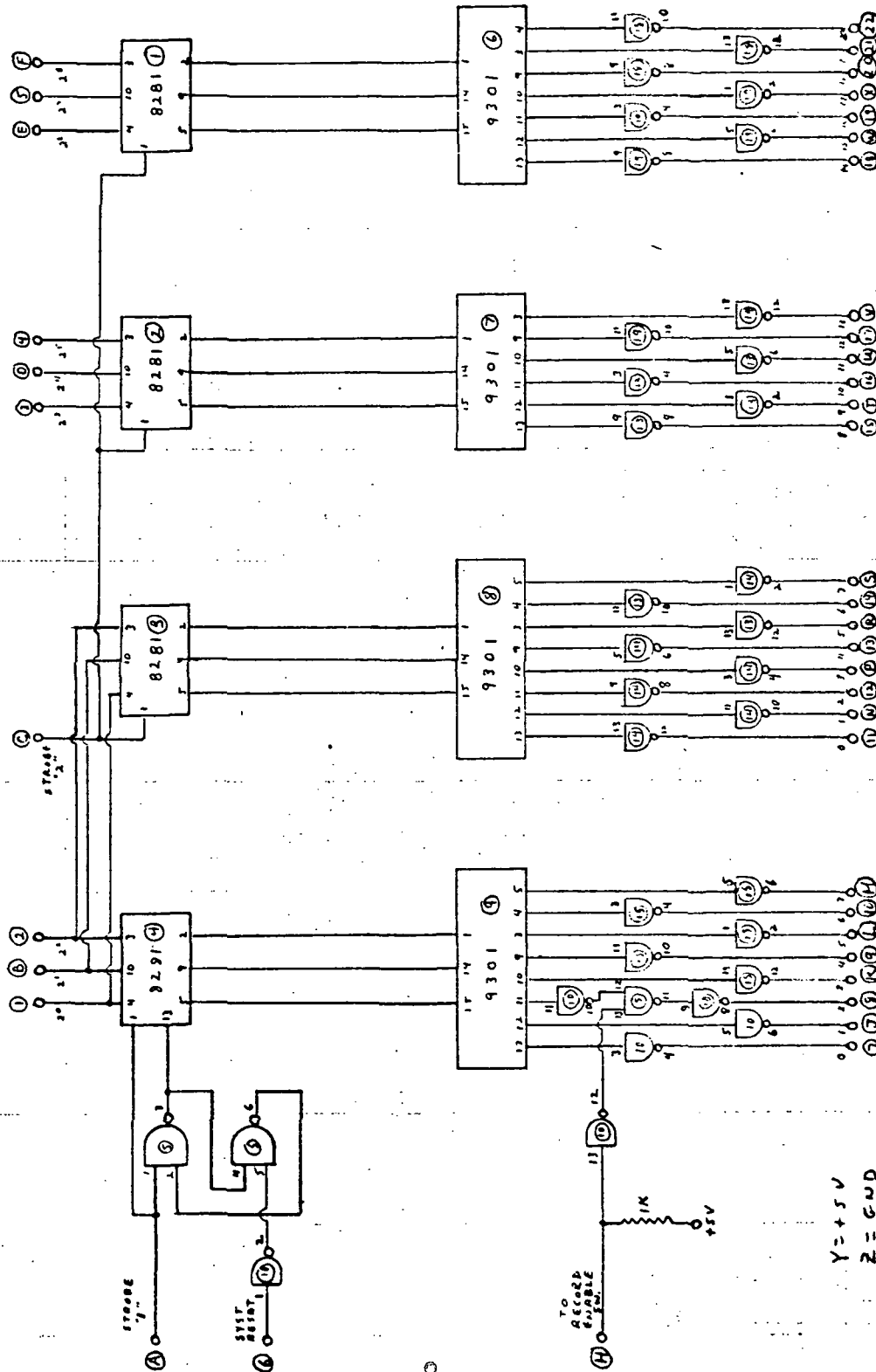


FIGURE 31. ANALOG TAPE RECORDER CONTROL (C1)

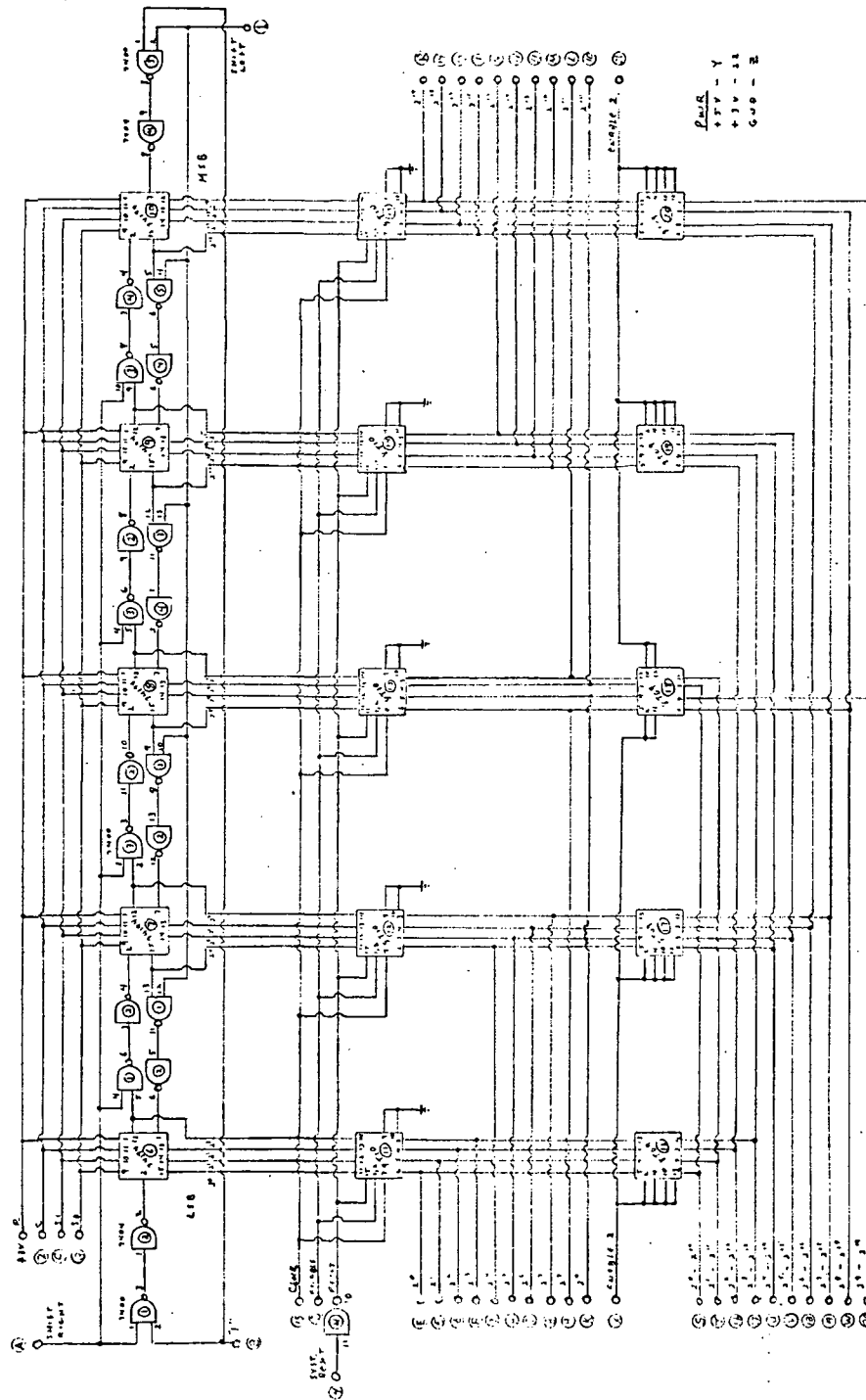


FIGURE 32. ANALOG LINE-COUNT DECODER (C2)

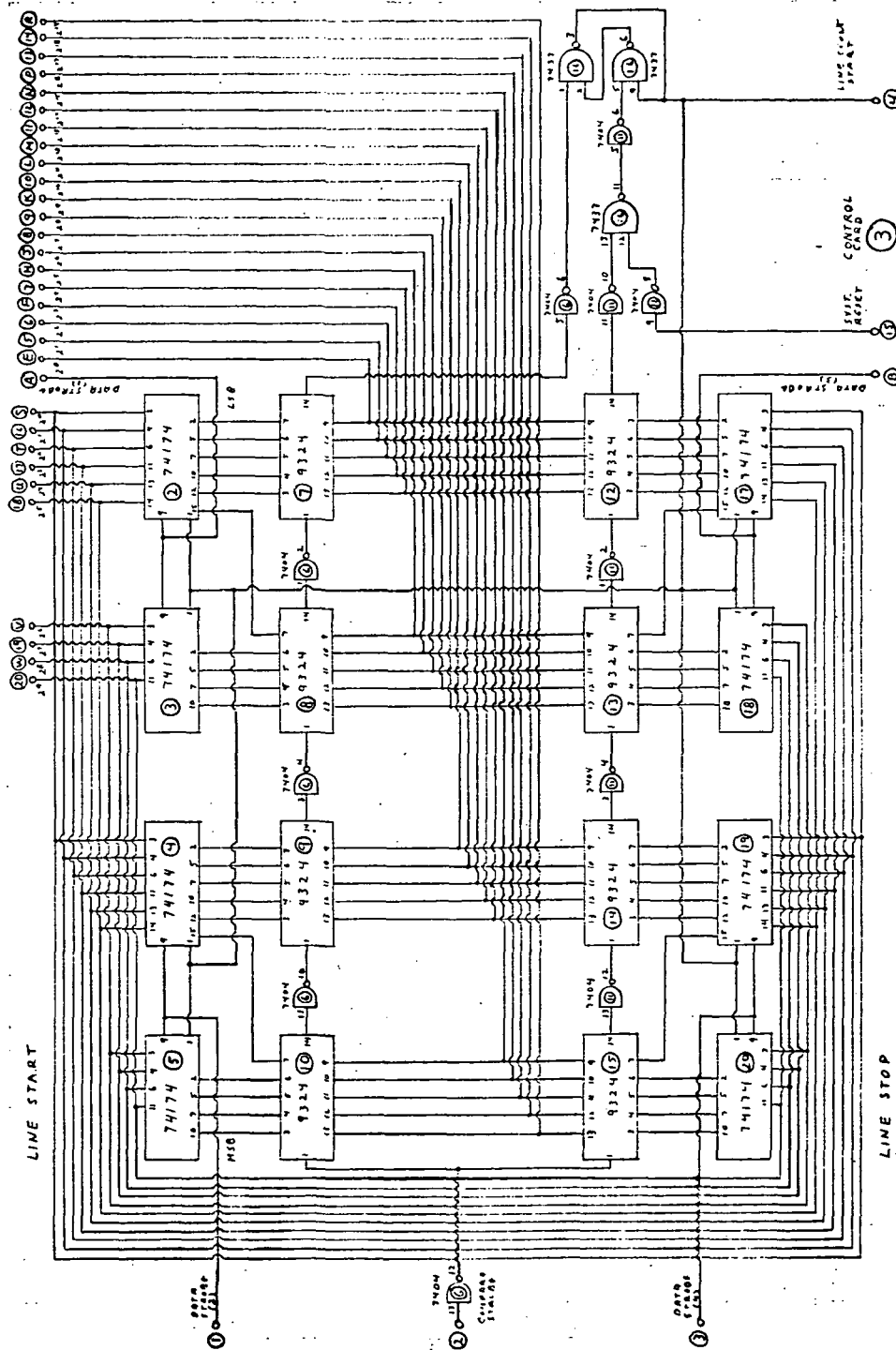
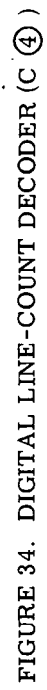


FIGURE 33. LINE-COUNT START/STOP (C 3)



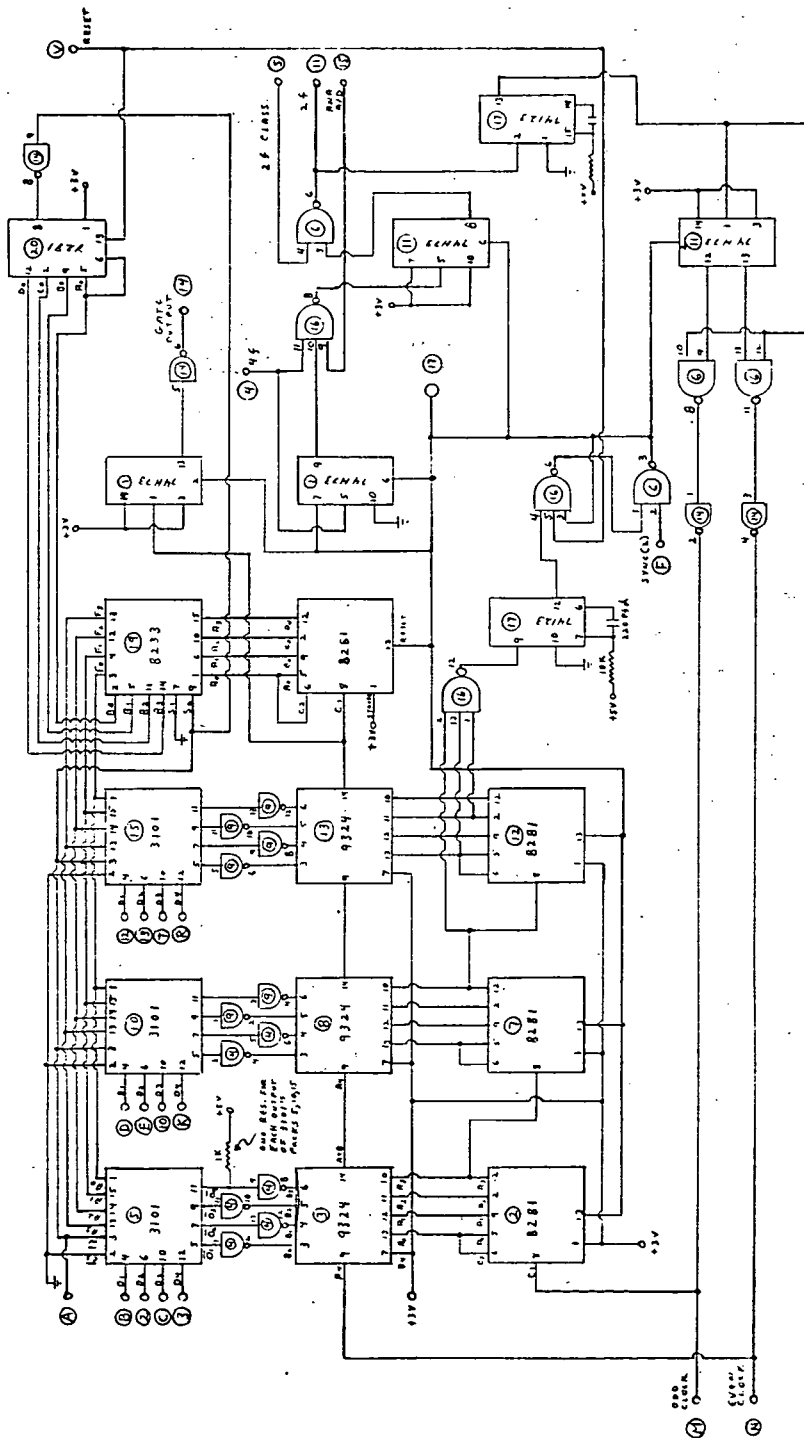


FIGURE 35. VIDEO AND CALIBRATION GENERATOR (C 6.7)

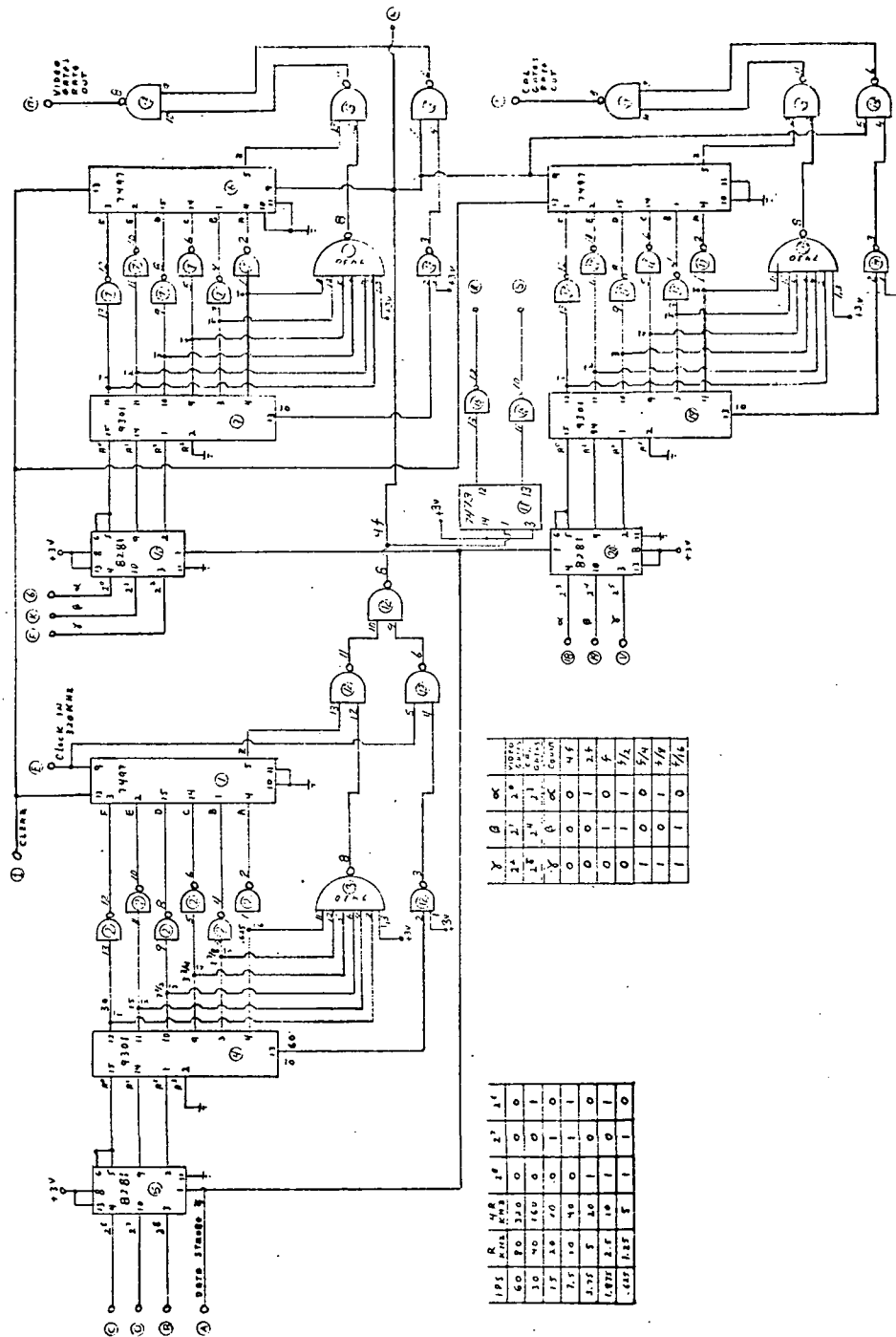
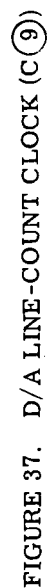


FIGURE 36. A/D-D/A CLOCK GENERATOR (C 8)



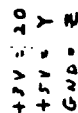
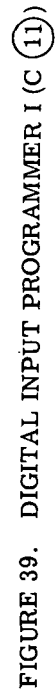


FIGURE 38. D/A DUTY CYCLE GENERATOR (C 10)





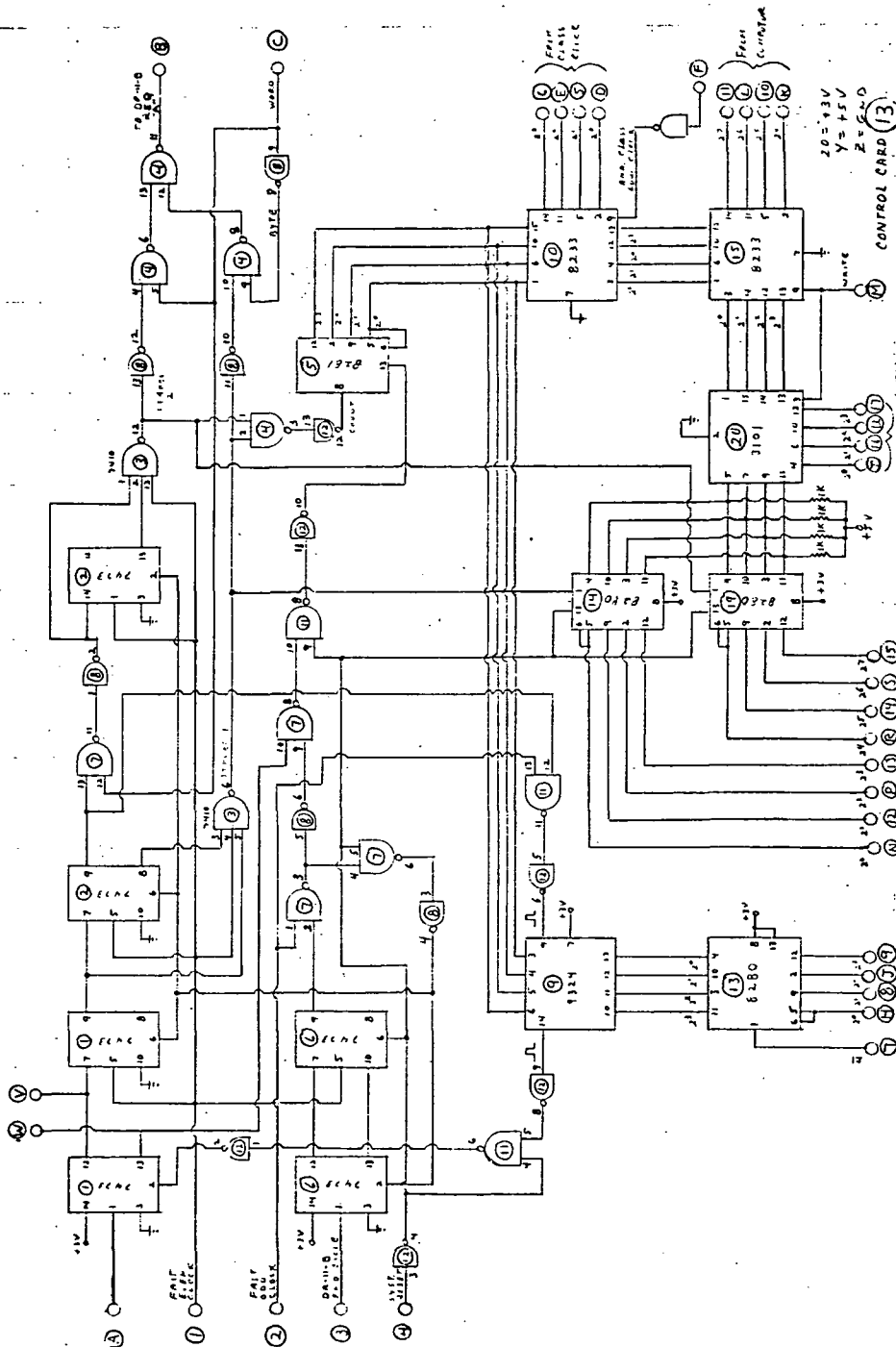


FIGURE 41. DIGITAL OUTPUT PROGRAMMER I (C 13)



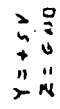


FIGURE 43. SYSTEM CONDITIONER I (C 15)

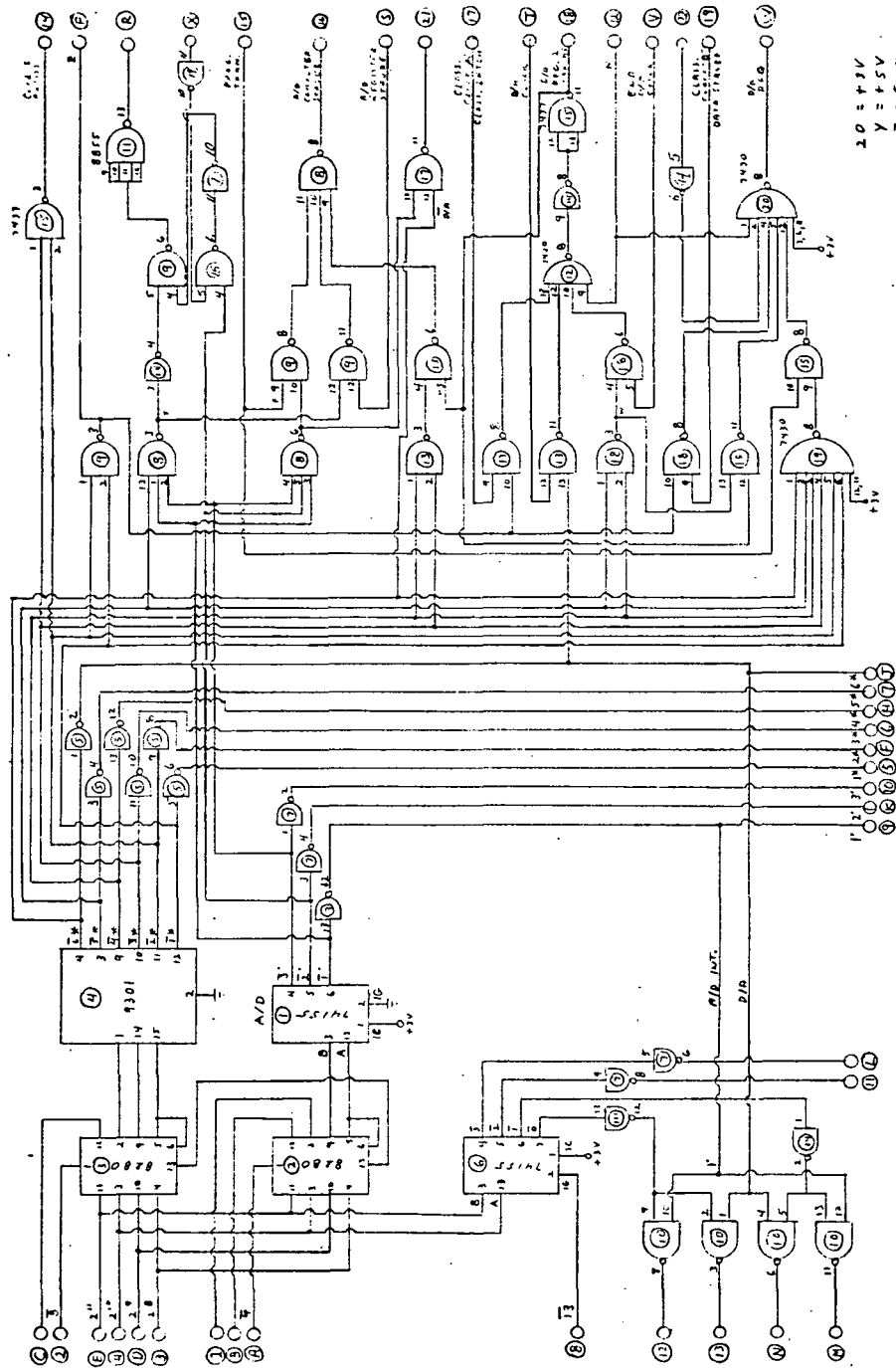


FIGURE 44. SYSTEM CONDITIONER II (C 16)

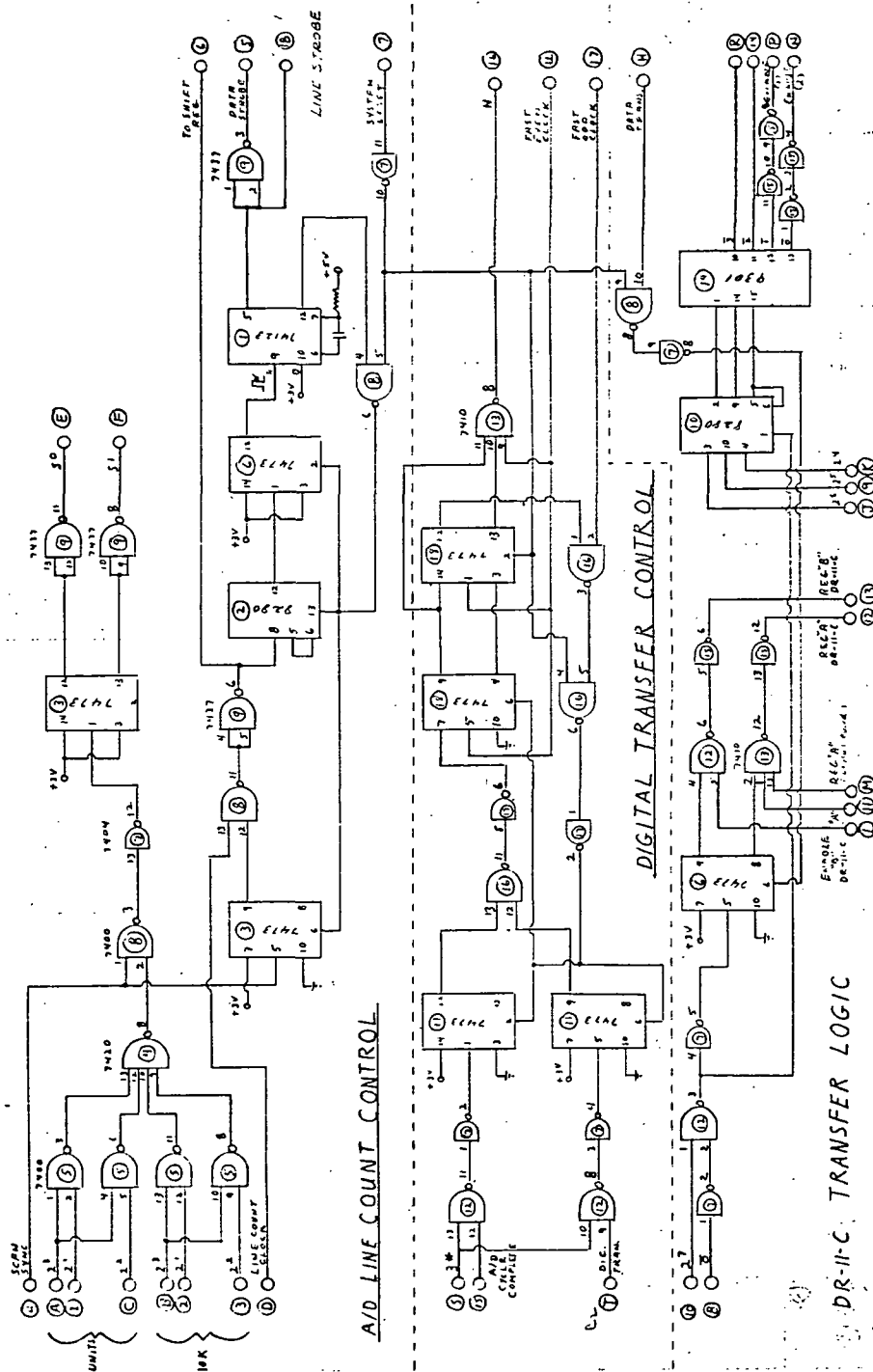


FIGURE 45. A/D LINE-COUNT CONTROL, DIGITAL TRANSFER CONTROL, AND DR-11C TRANSFER LOGIC (C 17)

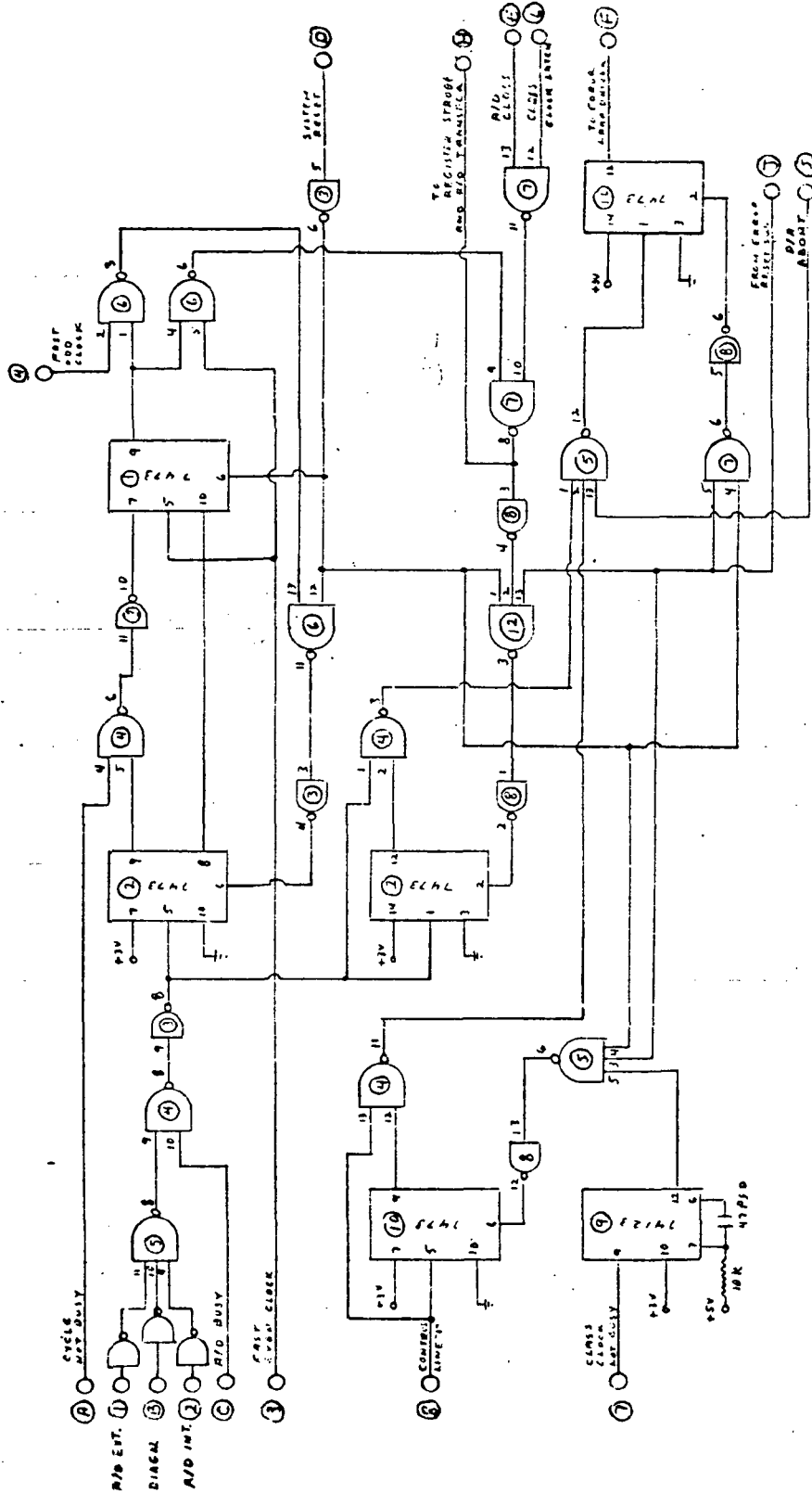


FIGURE 46. A/D WORD TRANSFER (C 18)

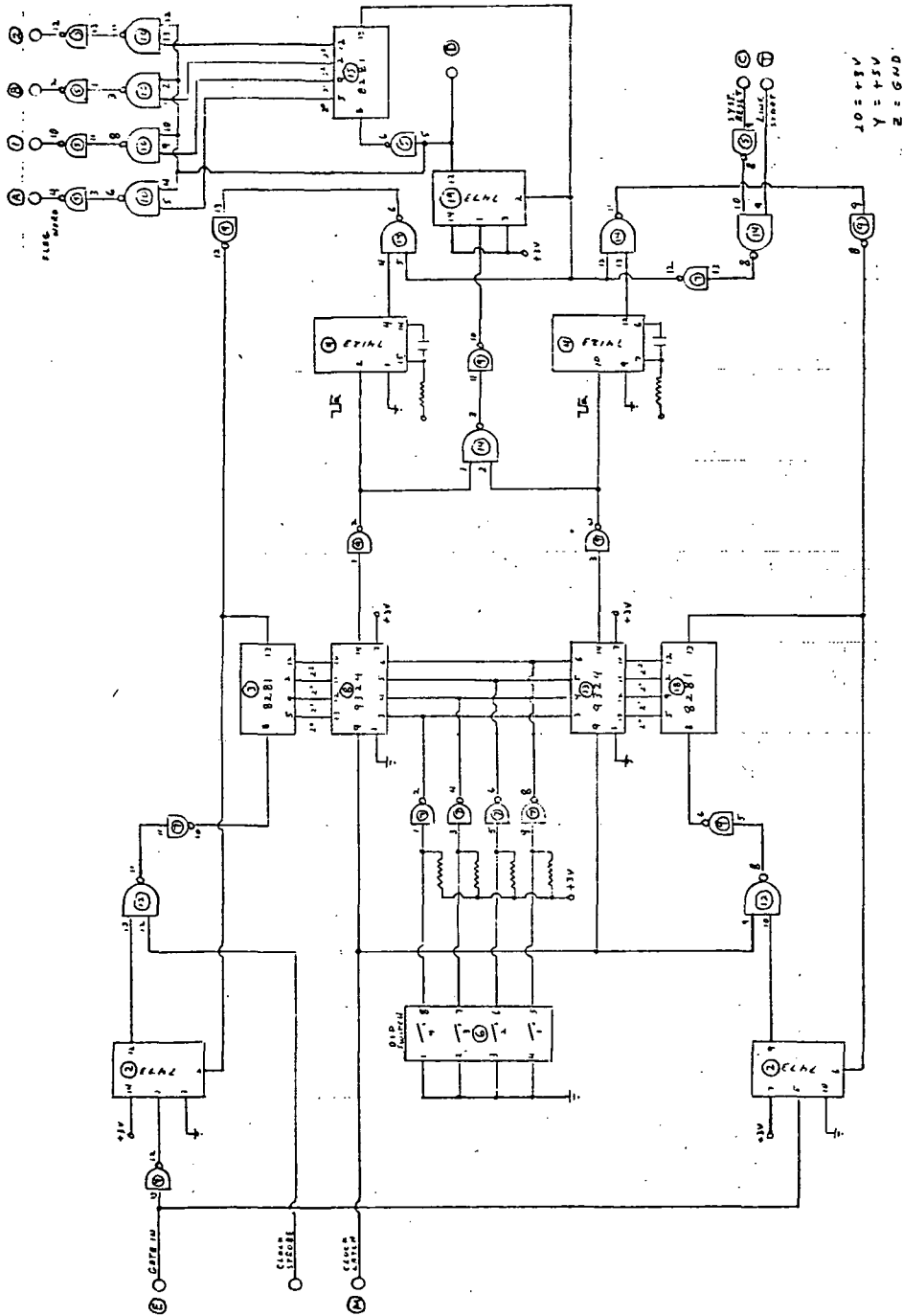
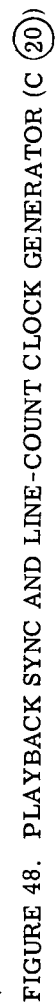


FIGURE 47. DELAY-GATE GENERATOR (C 19)



5

BACKPLANE INTRA-BAY WIRING

The wirewrap card files have backplanes with wirewrap connectors. These back-bay connectors have 122 pins, of which 10 are used for power and 10 for ground. Connections are shown in Fig. 49. Signal origins are shown by arrows. The various card locations are designated by odd numbers 1, 3, . . . , 25.

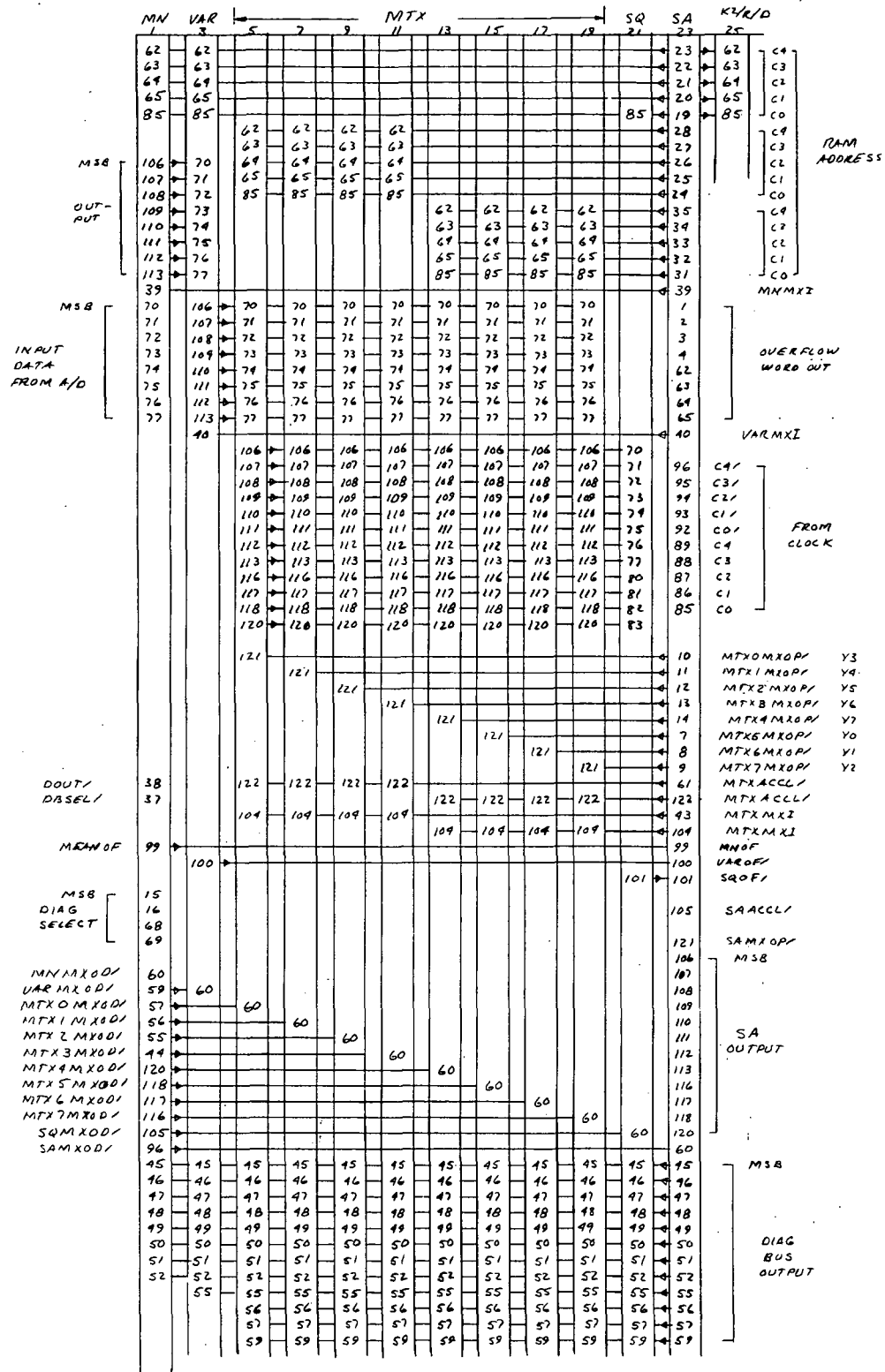


FIGURE 49. BACKPLANE INTRA-BAY WIRING (Continued)

	MN	VAR	MTX	1	2	3	4	5	6	7	SQ	SA	KZ
	1	3	5	7	9	11	13	15	17	19	21	23	25
MSB	1	1	1	1	1	1	1	1	1	1			1
DIFFERENTIAL	2	2	2	2	2	2	2	2	2	2			2
RAM	3	3	3	3	3	3	3	3	3	3			3
CONSTANTS	4	4	4	4	4	4	4	4	4	4			4
	7	7	7	7	7	7	7	7	7	7			7
	8	8	8	8	8	8	8	8	8	8			8
	9	9	9	9	9	9	9	9	9	9			9
	10	10	10	10	10	10	10	10	10	10			10
	11	11											11
	12	12											12
	13	13											13
	14	14											14
CS	98	98	98	98	98	98	98	98	98	98			98
VARRD	20	97											
MTX0 RRD	21		97										
MTX1 RRD	22			97									
MTX2 RRD	23				97								
MTX3 RRD	24					97							
MTX4 RRD	25						97						
MTX5 RRD	26							97					
MTX6 RRD	27								97				
MTX7 RRD	28									97			
MN RRD	97												
KZ/CHI RRD	40												97
LN RRD	43												99
												68	68
													8CHAN
MSB	80												
RAM	81												
CONSTANTS	82												
INPUT	83												
	84												
	86												
	87												
	88												
	89												
	93												
	94												
	95												
MSB	31										106		
RAM SEL	32										107	70	
INPUT	33										108	71	
	34										109	72	
RBAYSEL	35										110	73	
READ	36										111	74	
											112	75	
											113	76	
											114	77	
											117	80	
											118	81	
											120	82	
											105	83	
	115	115	115	115	115	115	115	115	115	115	115	115	
	103	103	103	103	103	103	103	103	103	103	103	103	
	91	91	91	91	91	91	91	91	91	91	91	91	
	79	79	79	79	79	79	79	79	79	79	79	79	
	67	67	67	67	67	67	67	67	67	67	67	67	
	59	59	59	59	59	59	59	59	59	59	59	59	
	42	42	42	42	42	42	42	42	42	42	42	42	
	30	30	30	30	30	30	30	30	30	30	30	30	
	18	18	18	18	18	18	18	18	18	18	18	18	
	6	6	6	6	6	6	6	6	6	6	6	6	
	114	114	114	114	114	114	114	114	114	114	114	114	
	102	102	102	102	102	102	102	102	102	102	102	102	
	90	90	90	90	90	90	90	90	90	90	90	90	
	78	78	78	78	78	78	78	78	78	78	78	78	
	66	66	66	66	66	66	66	66	66	66	66	66	
	53	53	53	53	53	53	53	53	53	53	53	53	
	41	41	41	41	41	41	41	41	41	41	41	41	
	29	29	29	29	29	29	29	29	29	29	29	29	
	17	17	17	17	17	17	17	17	17	17	17	17	
	5	5	5	5	5	5	5	5	5	5	5	5	

(b) Sheet 2
FIGURE 49. BACKPLANE INTRA-BAY WIRING (Concluded)

6 SYSTEM CABLING

6.1 CABLING BETWEEN HYBRID AND CONTROL BAYS

The wiring for data and control signals flows between the hybrid and control bays including PC-board card plugs that terminate the cables interconnecting the bays. One end of each printed circuit board accommodates cable wires at tie points (T.P.) on the card; the other end of the PC board has a printed circuit connector that mates with a card slot in the connector housing associated with a particular bay.

The connector housings comprise two auxiliary files located at the rear of the control and hybrid bays, respectively. In each of these files are four card slots for the card plugs of the cables. Each slot is assigned a number (1 through 4) and a code letter (C or H) to give its position in the file and identify that file with one of the two bays (control or hybrid). Figure 50 shows overall system cabling; the table below lists the terminations of the cables that originate in the two auxiliary files.

<u>SLOT in Aux. File</u>		<u>TERMINATION</u>
Control Bay	1-C	MIDAS CLASSIFIER
	2-C	2-H
	3-C	CONTROL PANEL
	4-C	DR-11C INTERFACE
Hybrid Bay	1-H	DR-11B INTERFACE
	2-H	2-C
	3-H	BNC CONNECTOR PANEL
	4-H	BNC CONNECTOR PANEL

The description of the interconnecting cables to and from the bays is given in Figs. 51 to 60; these figures detail the card plugs and also further describe the termination of the cables that tie into the auxiliary card files. As indicated in these diagrams, certain of the signals are buffered on the card plugs by line drivers (8T13) and line receivers (8T14). From Fig. 50 we see that cable 1C terminates eventually at the classifier. This is via a card plug that mates with a standard DEC block; then from the DEC block the signals are brought to the classifier using point-to-point wirewrap. Figure 55 shows the layout of the card plugs associated with the DEC block while Fig. 56 gives the block configuration. It may be noted that the cables originating from slots 3-H and 4-H are not detailed in this section.

6.2 CABLING BETWEEN CLASSIFIER AND COMPUTER

As indicated in the system cabling diagram (Fig. 50), a cable runs from the classifier to a DR-11B interface; it is used to carry information (e.g., RAM load, classifier output, diagnostic info) to and from the classifier through the DEC block. At the classifier end, this cable terminates in a card plug which connects to a DEC block (for block layout, see Fig. 56). The classifier

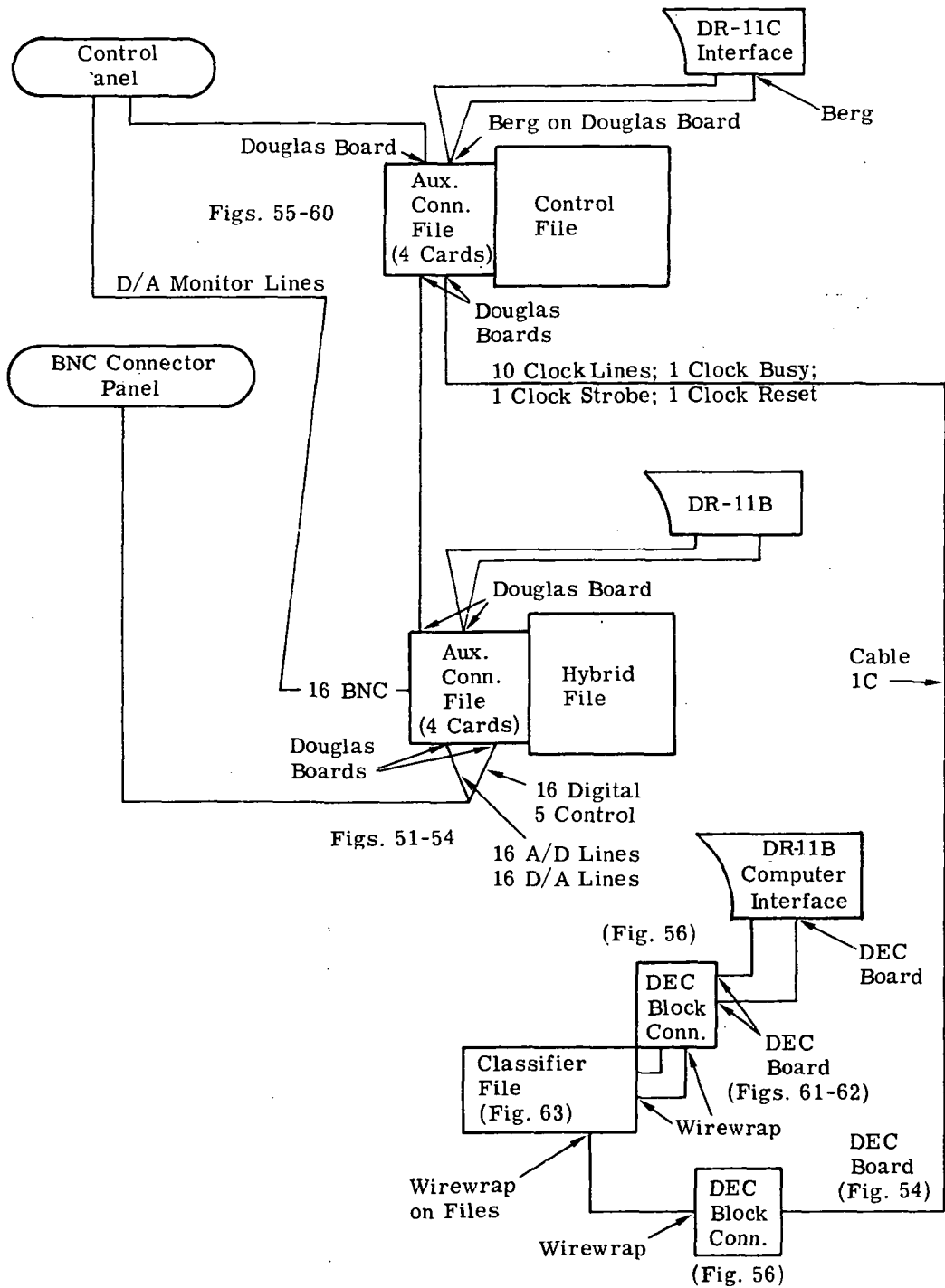


FIGURE 50. SYSTEM-CABLING DIAGRAM

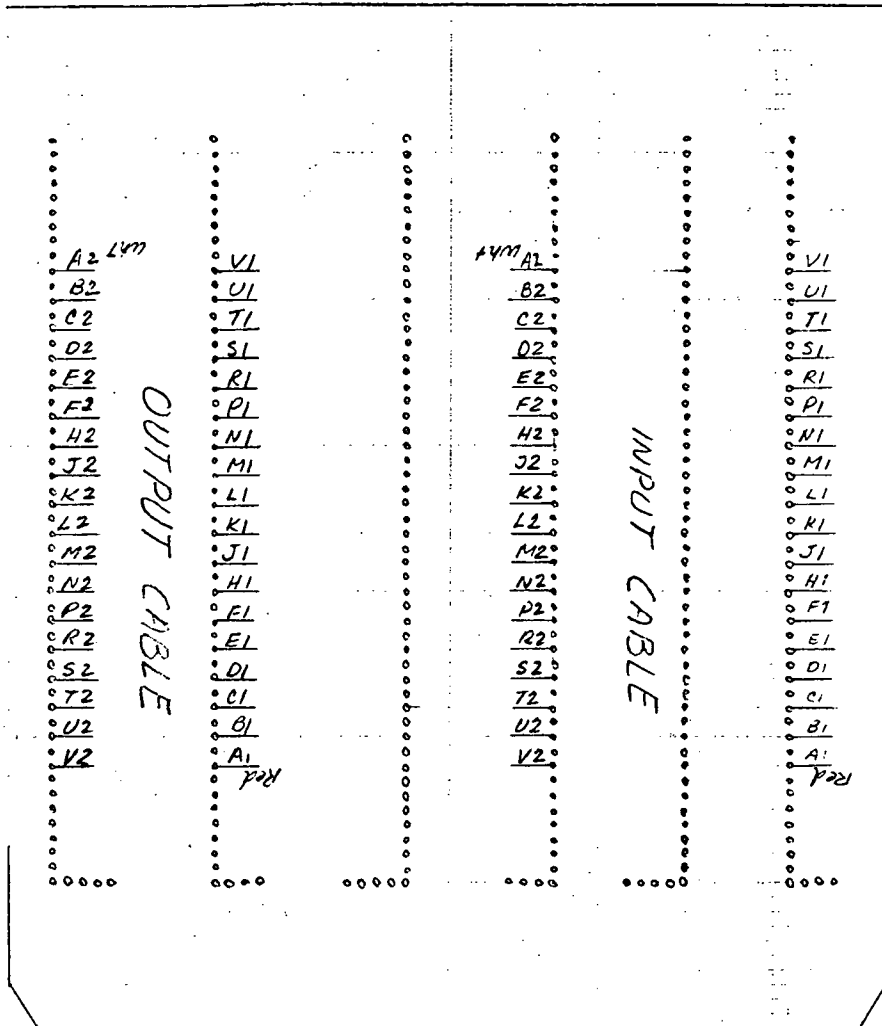


FIGURE 51. PHYSICAL LAYOUT OF PLUG CARD 1-H

DR-11B Input Cable			DR-11B Output Cable		
No.	Pin	Connector	No.	Pin	Connector
1.	A1	A	1.	V1	N
2.	B1	1	2.	F2	12
3.	C1	B	3.	H1	P
4.	D1	2	4.	H2	13
5.	D2	C	5.	J2	R
6.	E1	3	6.	K1	14
7.	E2	D	7.	K2	S
8.	F1	4	8.	L1	15
9.	F2	E	9.	L2	T
10.	H1	5	10.	M1	16
11.	H2	F	11.	M2	U
12.	J1	6	12.	N1	17
13.	J2	H	13.	N2	V
14.	K1	7	14.	P1	18
15.	K2	J	15.	P2	W
16.	L2	8	16.	R1	19
17.	M1	K	17.	R2	X
18.	M2	9	18.	S1	20
19.	N2	L	19.	S2	Y
20.	S2	10	20.	T2	21
21.	T1	M	21.	U1	Z
22.	U2	11	22.	U2	22
Function			Function		
Cycle Request A			(GO)		
End Cycle Out			C1 Control		
Data 00			Function 2		
Data 01			Single Cycle		
Data 02			Function 3		
Data 03			Data 11		
Data 04			Data 15		
Data 05			Data 09		
Data 06			Data 14		
Data 07			Data 07		
Data 08			Data 13		
Data 09			Data 05		
Data 10			Data 12		
Data 11			Data 03		
Data 12			Data 10		
Data 13			Data 01		
ATTEN.			Data 08		
Data 14			Data 00		
Data 15			Data 06		
Busy			Data 04		
GND			Cycle Request B		
INIT.			Data 02		

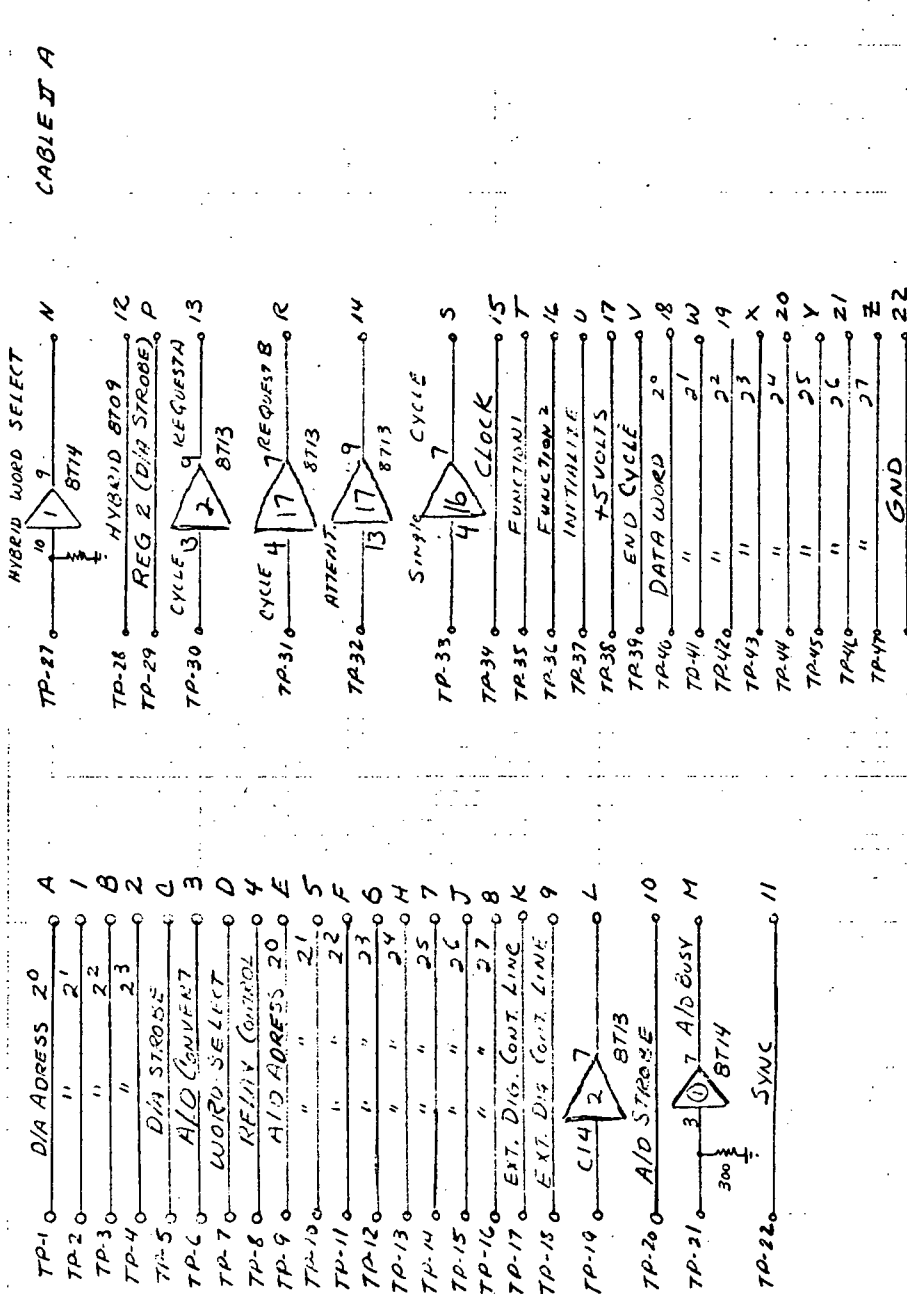
Note: Gnd. (T1) on both input and output cable to card.

Note: Gnd (F1) and output cable to gnd on card.

Figure (a)

Figure (b)

FIGURE 52. OUTPUT CONNECTOR WIRING OF PLUG CARD (1-H)



NOTE: GND CARRIED SEPARATELY FROM
FLAT CABLE
PIN 22 TO GND BUS ON CARD

FIGURE 53. WIRING OF PLUG CARD 2-H

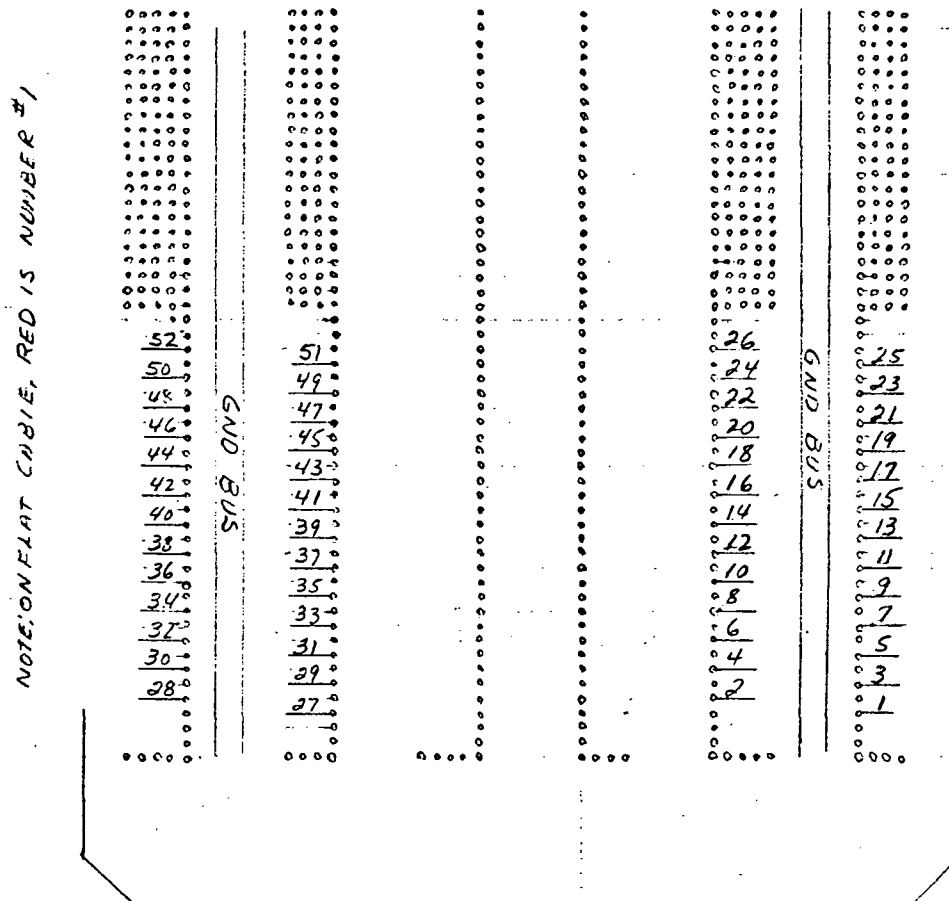
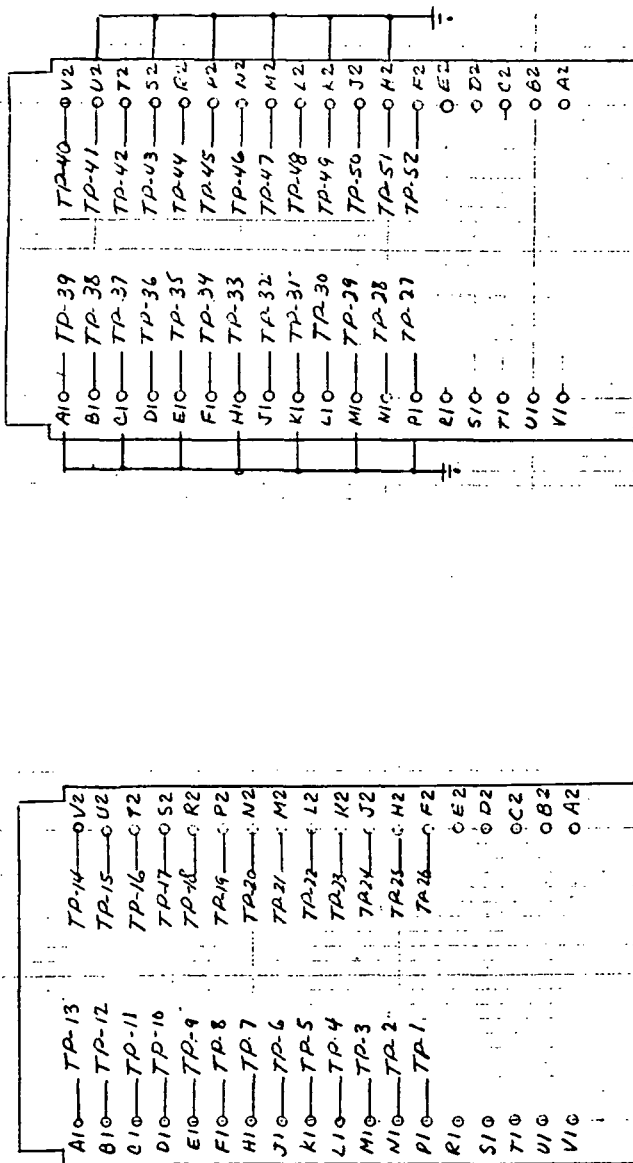


FIGURE 54. PHYSICAL LAYOUT OF PLUG CARDS (2-H) AND (2-C)





BLOCK 2-A
Pos 2.

NOTE: VIEW SHOWN
IS SOLDER LUGS UP

NOTE: TO DEC BLOCK-DESTINATION CLASSIFIER

(b) DEC Block Termination of Plug Card 1-C

FIGURE 55. PLUG CARD 1-C (Continued)

BLOCK CONNECTOR 2-A Position 2		BLOCK CONNECTOR 2-A Position 4	
A1 Gnd.	A2	A1 2 ⁰	Data Word A2
B1 Clock Busy	B2	B1 2 ¹¹	Data Format B2
C1 Gnd.	C2	C1 2 ¹⁰	Data Format C2
D1 C4	D2	D1 2 ⁹	Data Format D2
E1 Gnd.	E2	E1 2 ⁸	Data Format E2
F1 C3	F2 Clock Reset	F1 2 ⁷	Data Format F2
H1 Gnd.	H2 Gnd.	H1 2 ⁶	Data Format H2 Video
J1 C2	J2 Clock Strobe	J1 2 ⁵	Data Format J2 2 ³ Video Gate & Flag
K1 Gnd.	K2 Gnd.	K1 2 ⁴	Data Format K2 2 ² Video Gate & Flag
L1 C1	L2 Data Strobe	L1 2 ³	Data Format L2 2 ¹ Video Gate & Flag
M1 Gnd.	M2 Gnd.	M1 2 ²	Data Format M2 2 ⁰ Video Gate & Flag
N1 CØ	N2 C4	N1 2 ¹	Data Format N2 2 ⁷ Data Word
P1 Gnd.	P2 Gnd.	P1 2 ⁰	Data Format P2 2 ⁶ Data Word
R1	R2 C3	R1	2 ⁵ Data Word
S1	S2 Gnd.	S1	2 ⁴ Data Word
T1	T2 C2	T1	2 ³ Data Word
U1	U2 Gnd.	U1	2 ² Data Word
V1	V2 C1	V1	2 ¹ Data Word

(c) Connector Wiring of DEC Block Termination

FIGURE 55. PLUG CARD (1-C) (Concluded)

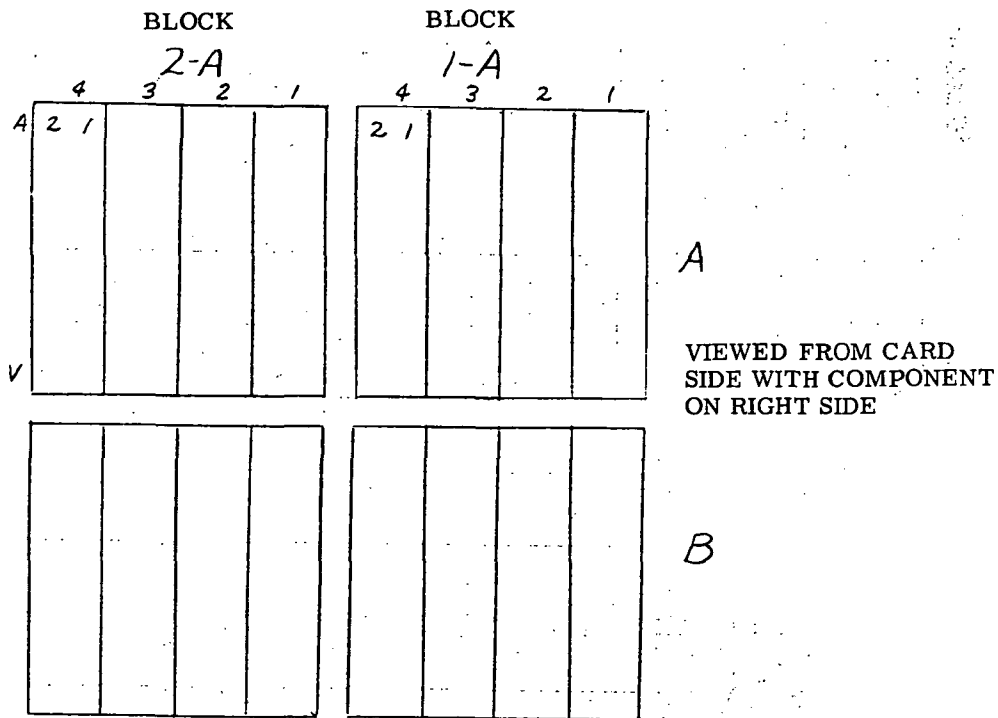
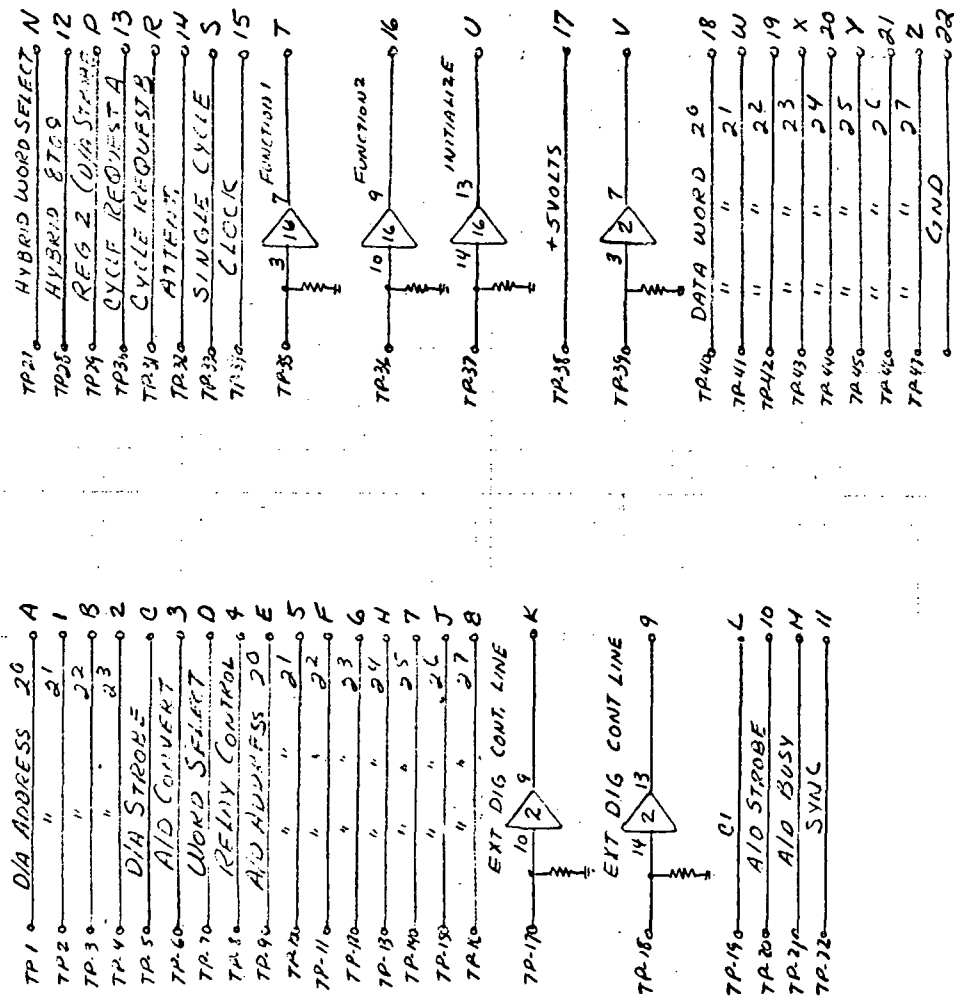


FIGURE 56. DEC BLOCK LAYOUT

CABLE 11 8





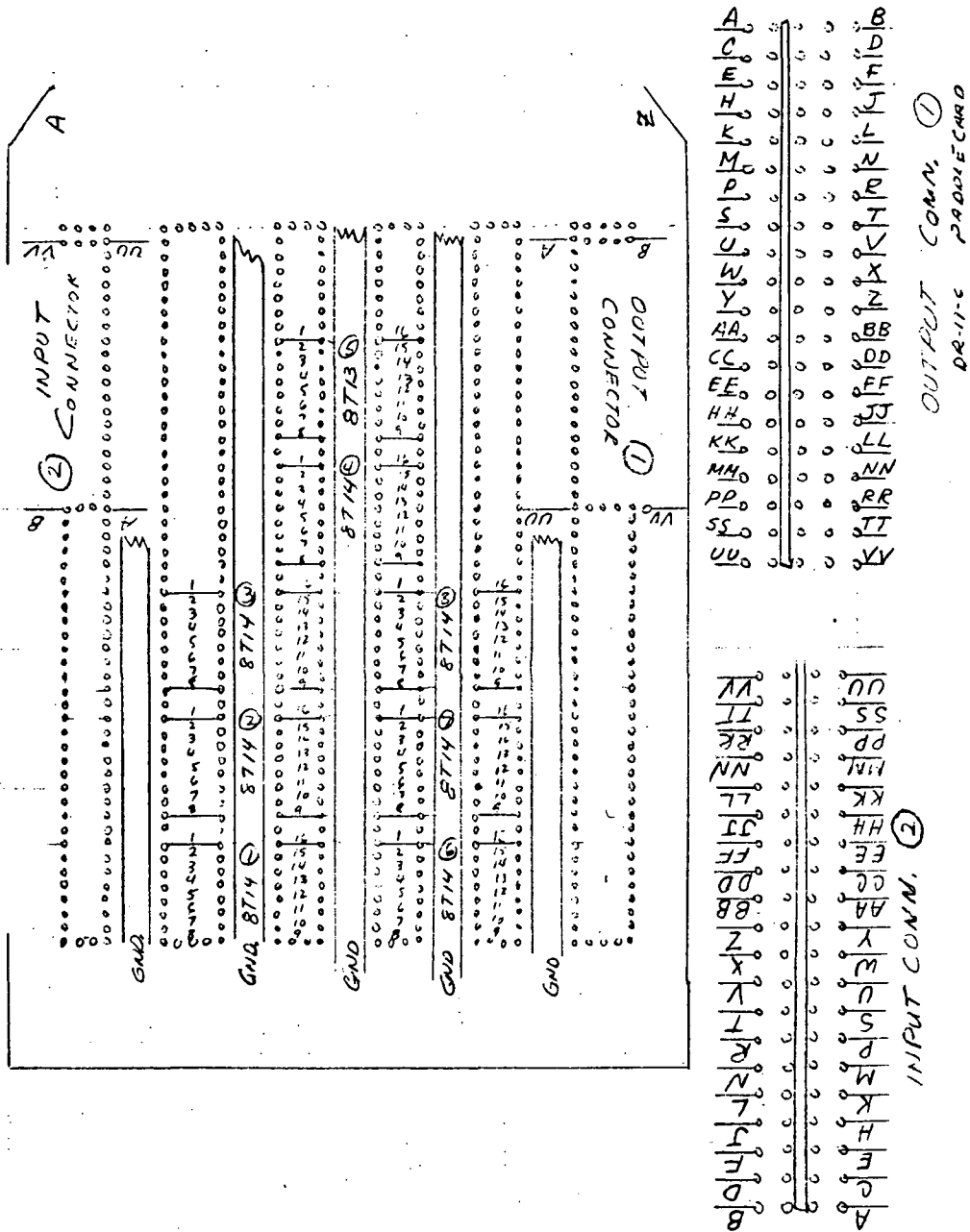


FIGURE 59. PHYSICAL LAYOUT OF PLUG CARD (4-C)

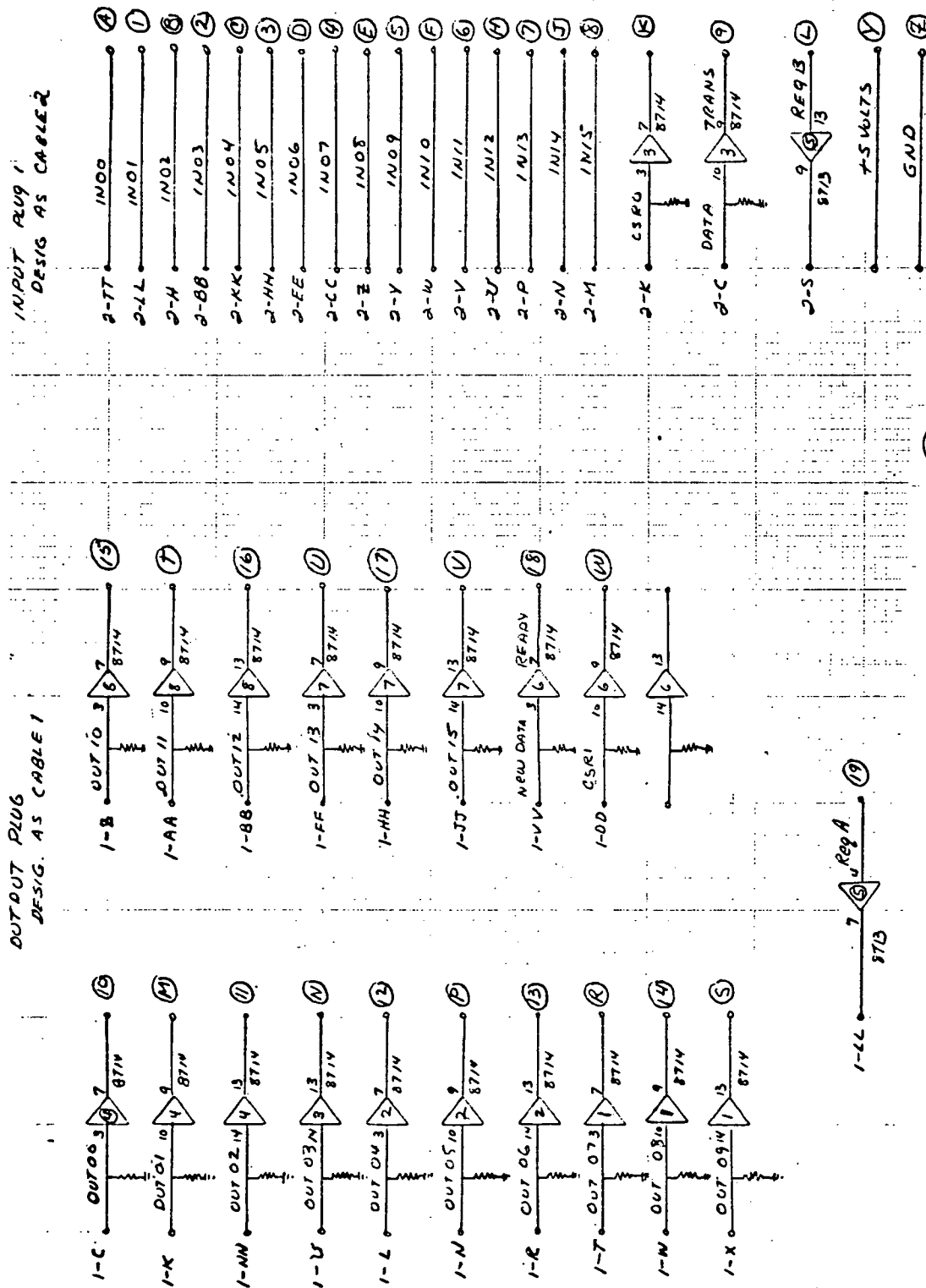
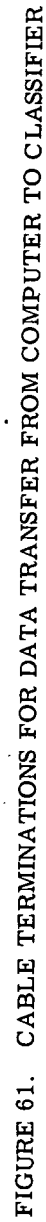


FIGURE 60. WIRING OF CARD 4-C

connection to the computer via the DR-11B is through line drivers and receivers located on the card plugs; these cards are detailed in Figs. 61 and 62. The classifier inter-bay wiring and cabling to the DEC block are shown in Fig. 63.



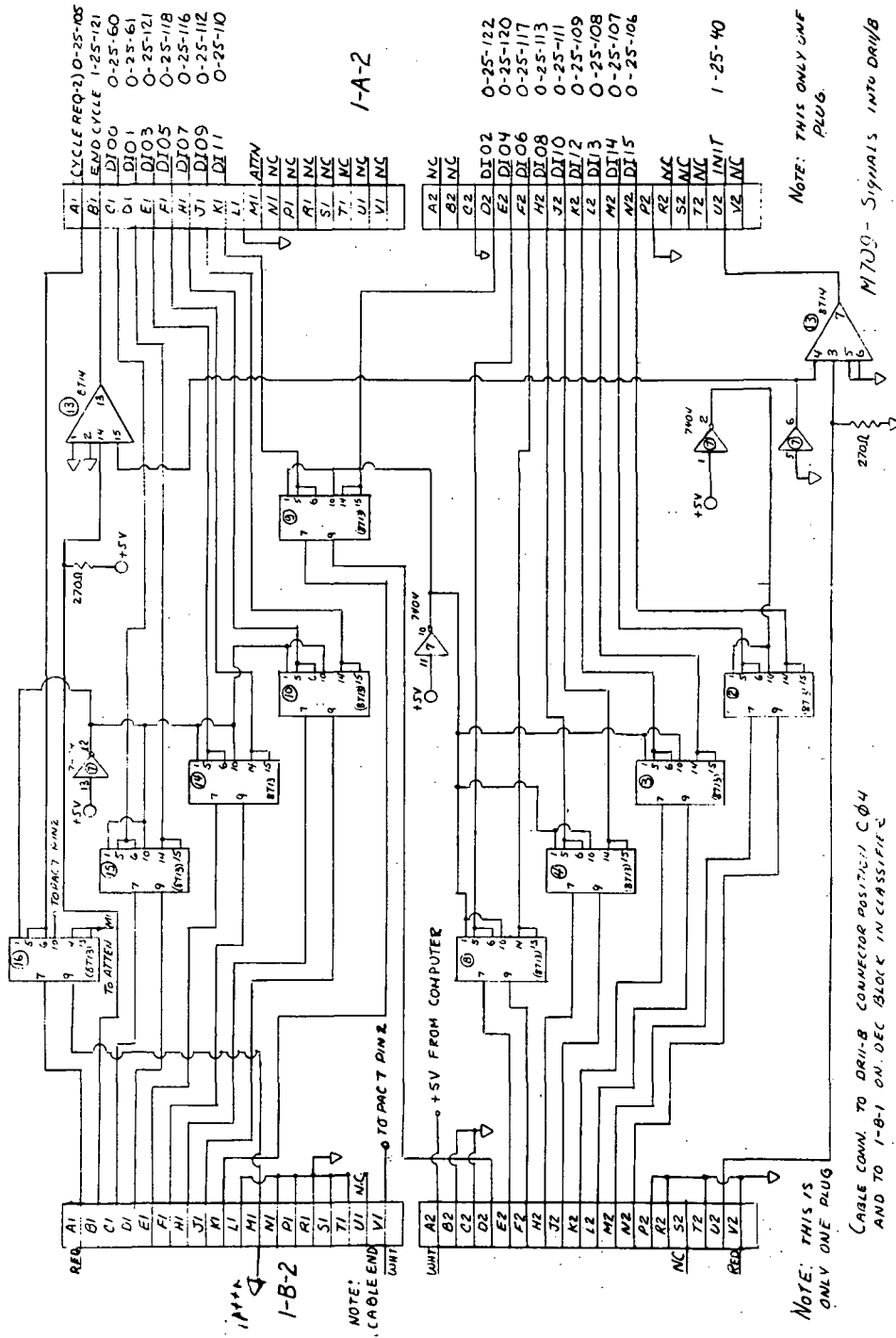
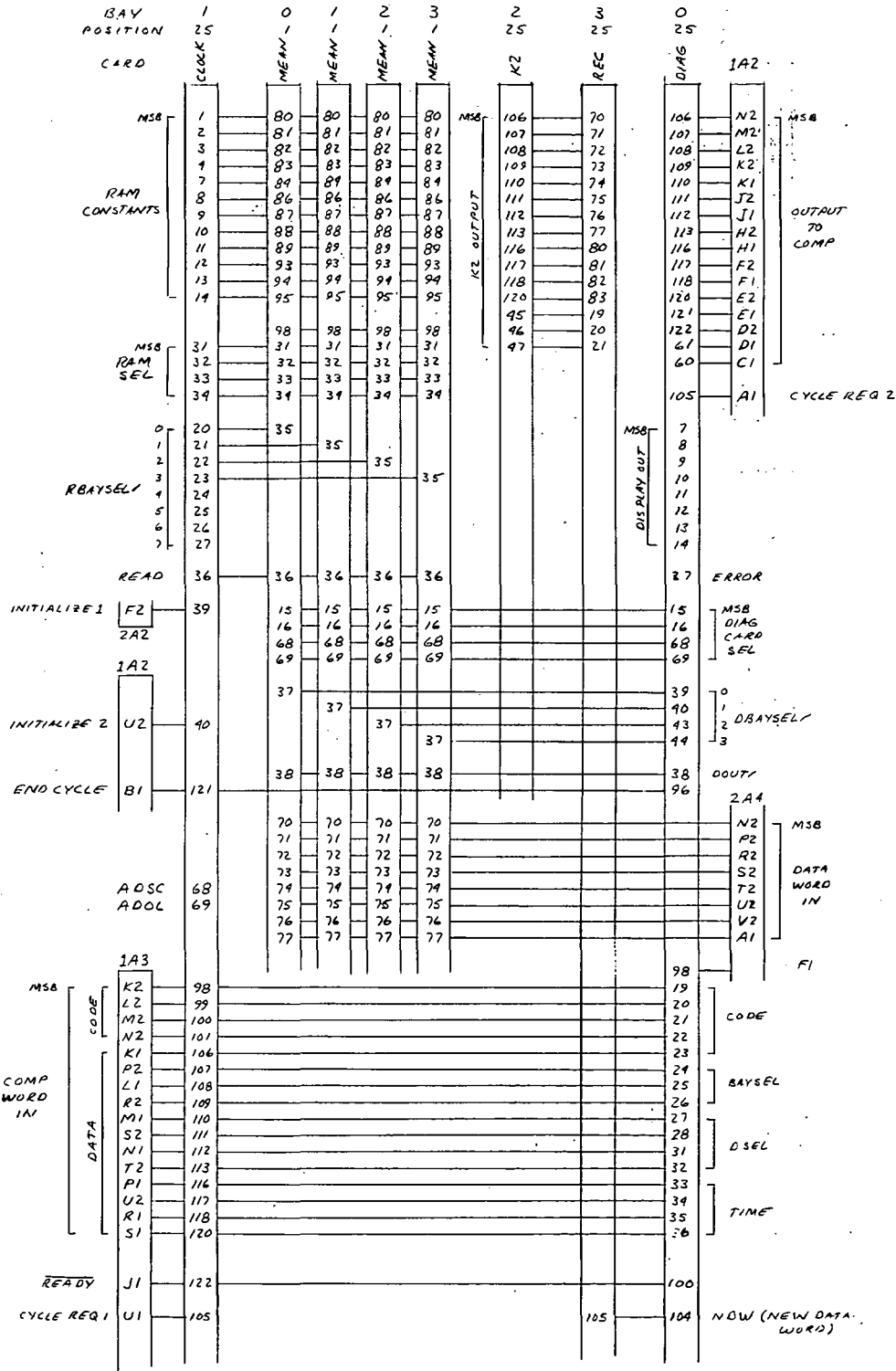
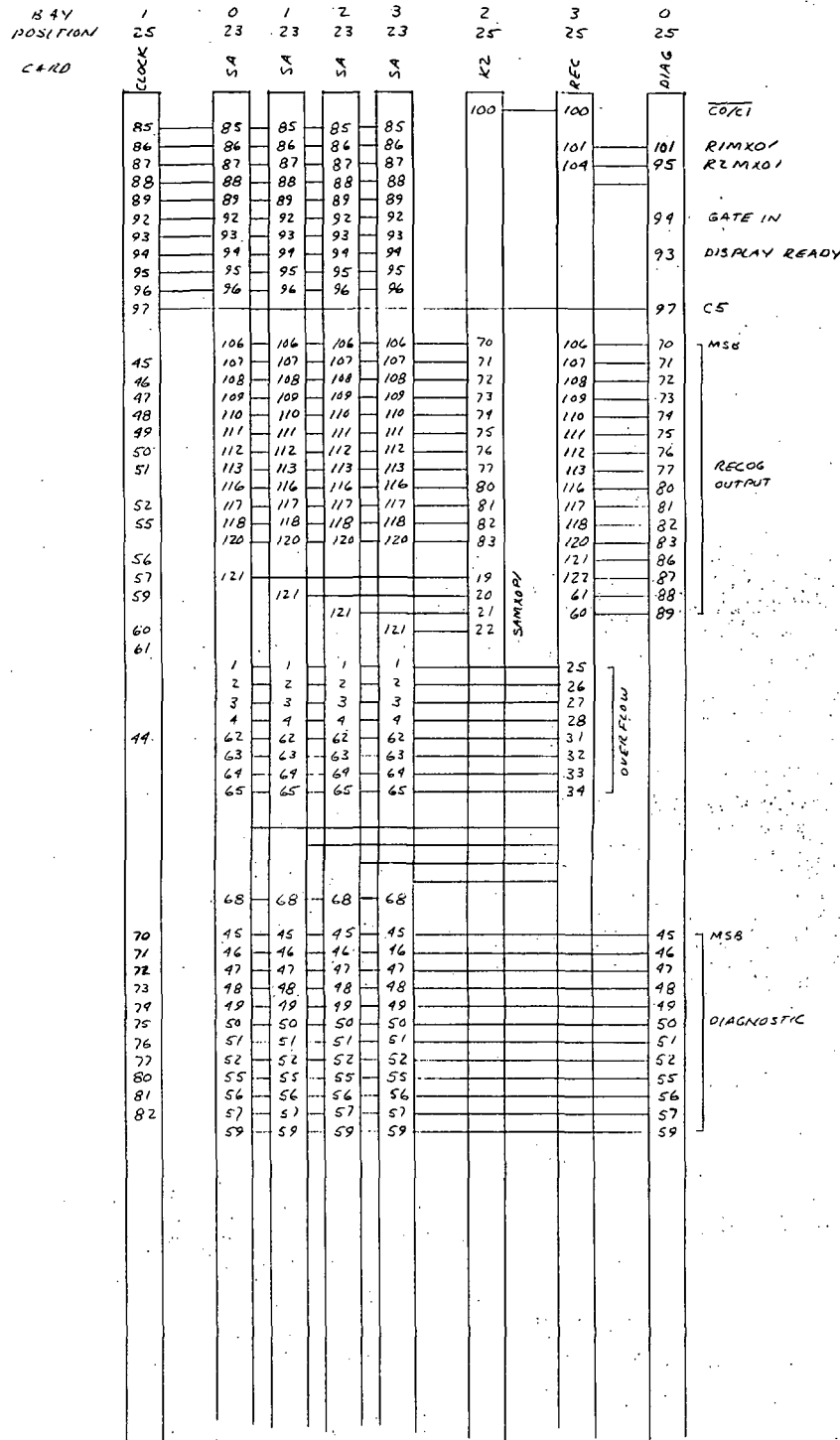


FIGURE 62. CABLE TERMINATIONS FOR DATA TRANSFER TO COMPUTER FROM CLASSIFIER



(a) Sheet 1
FIGURE 63. INTER-BAY WIRING (Continued)



(b) Sheet 2
FIGURE 63. INTER-BAY WIRING (Concluded)

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